MONOPULSE BEACON TEST SET (MBTS)

SYSTEM OPERATIONS/TRAINING MANUAL

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A	Original Release	March 18, 2002
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Title: President
Date: July 11, 2003

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1 GENERAL INFORMATION

1.1 About This Training Manual

This interactive training manual is designed for viewing on a computer using Adobe Acrobat 4.0® or higher. It operates similar to an Internet browser and web page with hyperlinks.

Chapter 1 of this manual provides information about the use of this guide, and includes an overview of the MBTS equipment and the Operator Control Subsystem (OCS) software. Extensive links (shown in light blue) within the text, and associated with many of the figures, allow a user to quickly get detailed information about a selected item.

Chapter 2, System Operation, includes detailed information concerning the operation of the MBTS and the Operator Control Subsystem (OCS) software. All major MBTS Operational Modes are described.

Chapter 3, Technical Description, provides an overview of the function of all major components and modules within the MBTS. Links provide quick access to OCS screens, connector detail, and indicator information as described in other sections of the manual.

Chapter 4, Standards and Tolerances, provides system and interface level MBTS technical specifications. Section 4.2, MBTS Signal Interfaces, lists the electrical and mechanical characteristics of front and rear panel connectors J1 through J28.

Chapter 5, MAINTENANCE AND REPAIR, provides preventive, diagnostic, and corrective maintenance information.

Chapter 6, Installation, Integration, and Checkout, describes how to install and integrate the MBTS with a radar system.

1.2 Navigation Within This Manual

The manual first opens to the Table of Contents page. Adobe Acrobat® "Bookmarks" appear in a separate window on the left side of the screen.

1.2.1 Tables of Contents and Interactive Illustrations

An interactive , List of Figures, List of Tables, MBTS Front Panel, MBTS Rear Panel and OCS Screen Layout, allows quick movement to desired sections within the manual. Moving the cursor over a page number or link, and double clicking the pointer or mouse, loads the desired page.

1.2.2 Bookmarks

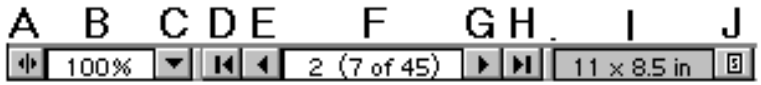
The "bookmarks" shown on the left of the screen provide a collapsible outline for this manual. When first opened, the outline is fully collapsed, showing only the main topics. Clicking on a plus [+] sign to the left of an entry expands the links under that entry. Clicking on a [-] sign to the left on an entry collapses the links under that entry. Moving the cursor over an entry highlights the line and expands it into the main window if it is longer than the window's width. Clicking on the entry with the pointer or mouse button opens that page in the main screen.

1.2.3 Links

This manual includes numerous text and graphics links to other areas within the manual. Links are always shown in light blue. Moving the cursor over a link and clicking on it, loads the new material.

1.2.4 Screen Control

A graphical menu similar to the one shown here is located at the bottom of the computer screen. The letters A through J, shown above the menu below, are keys to the function explanations.



A. This function allows re-sizing of the main window and the bookmark window. Place the cursor over Item A, hold down the left mouse button, and drag the item the left or right to resize the windows.

B. An indicator of the page size as it relates to an 11 x 8.5 inch sheet of paper.

C. Moving the cursor over Item C opens a pull-down menu. The menu includes a variety of standard magnification selections.

D. Clicking on Item D displays the opening page (cover sheet) of the manual.

E. Clicking on Item E moves the display one page back.

F. Item F shows the current page number and the page count within the manual. The Cover sheet has no page number. The manual's "front matter" is paginated in Roman Numerals. The main part of the manual is conventionally numbered. The numbers within parentheses show the actual page count, starting from the cover, plus the total number of pages in the manual.

G. Clicking on Item G displays the next page of the manual.

H. Clicking on Item H displays the very last page of the manual.

I. Area I indicates the size of the original page if printed.

J. Clicking on Item J opens a pull-down menu that determines the method of page transitions. The default is SINGLE, which is recommended, as it always displays one full page in the main window. CONTINUOUS allows continuous scrolling from one page to the next. CONTINUOUS FACING displays a matrix of the pages, much like "thumbnails" of the pages.

1.3 Overview of the Monopulse Beacon Test Set System

The Monopulse Beacon Test Set (MBTS) is designed to assist in the maintenance, certification, and test of the monopulse secondary surveillance radar (MSSR) systems within the FAA. These systems include the Air Traffic Control Beacon Interrogator, Model-6 (ATCBI-6), the Airport Surveillance Radar, Model-11 (ASR-11) MSSR, and the Mode Select (Mode S) Beacon Radar Systems. In addition, the MBTS may be used with existing ATCBI-5 and earlier, non-MSSR, systems.

The MSSR systems generate both Air Traffic Control Radar Beacon System (ATCRBS) and Mode S interrogations. In response to these, the MBTS generates reply signals that allow full characterization of ATCRBS and Mode S radar receiver performance, including the remote measurement of Overall System Sensitivity (OSS).

The MBTS generates continuous wave (CW) and pulsed RF signals. Pulsed signal target replies are created in response to either internal or external triggers, or in response to decoded radar interrogations. The MBTS uses azimuth position data derived from the radar system to calculate and synchronize the generation of target replies. Control of MBTS operation is via either a GPIB interface to a

dedicated Operator Control Subsystem (OCS) laptop computer or through a serial link to the ATCBI-6 system controller.

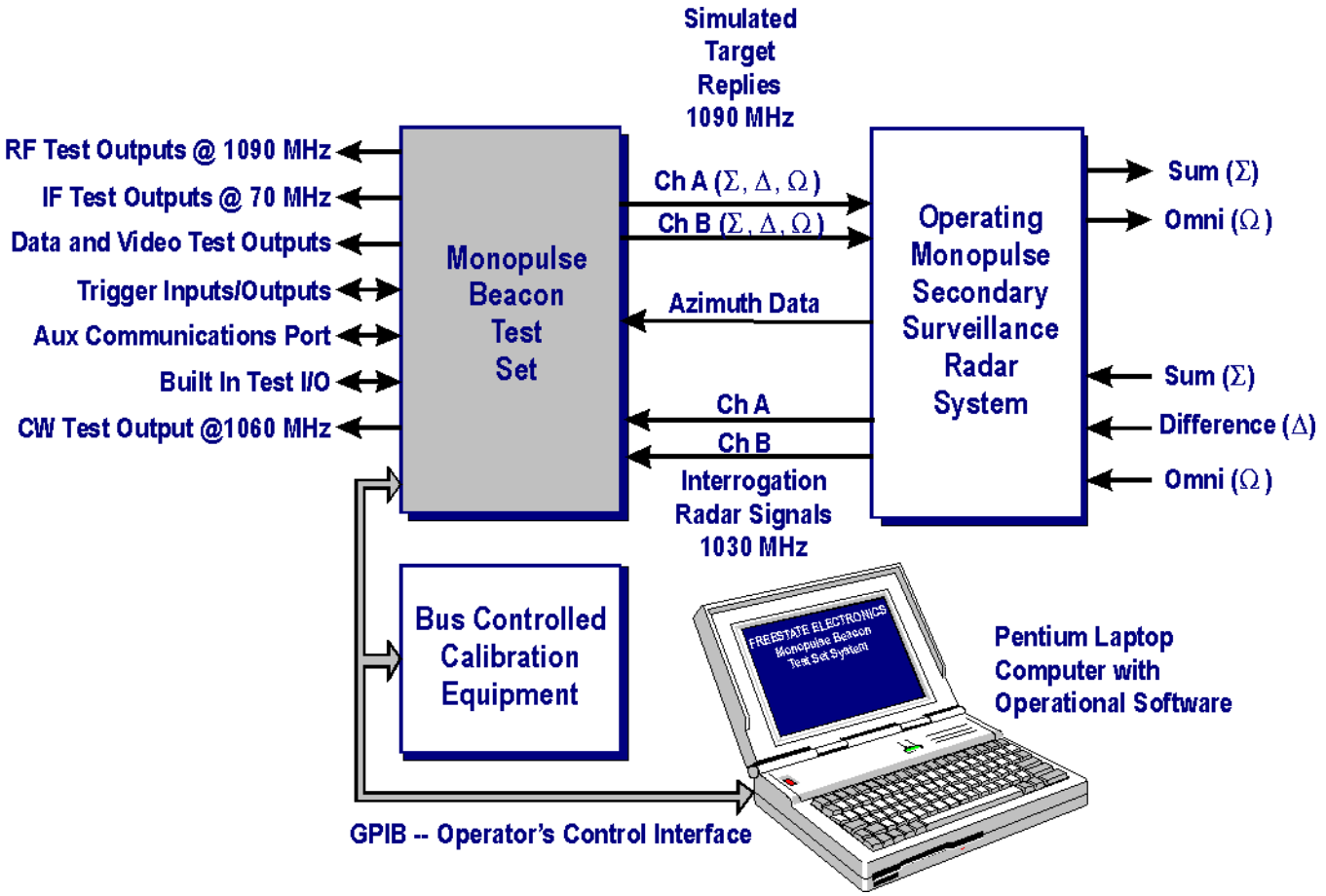
The MBTS includes all the functions required for the certification of MSSR system sensitivity and target detection. The MBTS also gives FAA field technicians the ability to test the MSSR from end-to-end, through the injection of ATCRBS or Mode S RF test targets into the MSSR receiver. MSSR test targets may then be observed at various points in the MSSR system, from the radar receiver inputs up to and including the controller's display. The primary functions of the MBTS include:

- Measuring and calibrating receiver sensitivity
- Measuring and calibrating fixed thresholds
- Measuring and calibrating Sensitivity Time Constant (STC) curves
- Measuring and calibrating delta/sum (Δ/Σ) thresholds
- Measuring and calibrating sum/omni (Σ/Ω) thresholds
- The test and alignment of the radar receiver system, using pulsed and CW signals

1.3.1 MBTS System Block Diagram

Figure 1, MBTS System Block Diagram, illustrates the general operational relationships between the top-level system components including the MBTS instrument and OCS controller, the operating Monopulse Secondary Surveillance Radar System, and auxiliary calibration or measurement equipment.

Figure 1. MBTS System Block Diagram



The MBTS system includes the MBTS unit, a Pentium based laptop computer running dedicated MBTS virtual instrument control software (the OCS), two sets of phase-matched RF cables, and an azimuth data cable. Power cords, IEEE-488 cables, IEEE-488 interface cards (part of the OCS), etc., are also delivered with the MBTS system.

1.3.2 Monopulse Beacon Test Set (MBTS) Physical Description

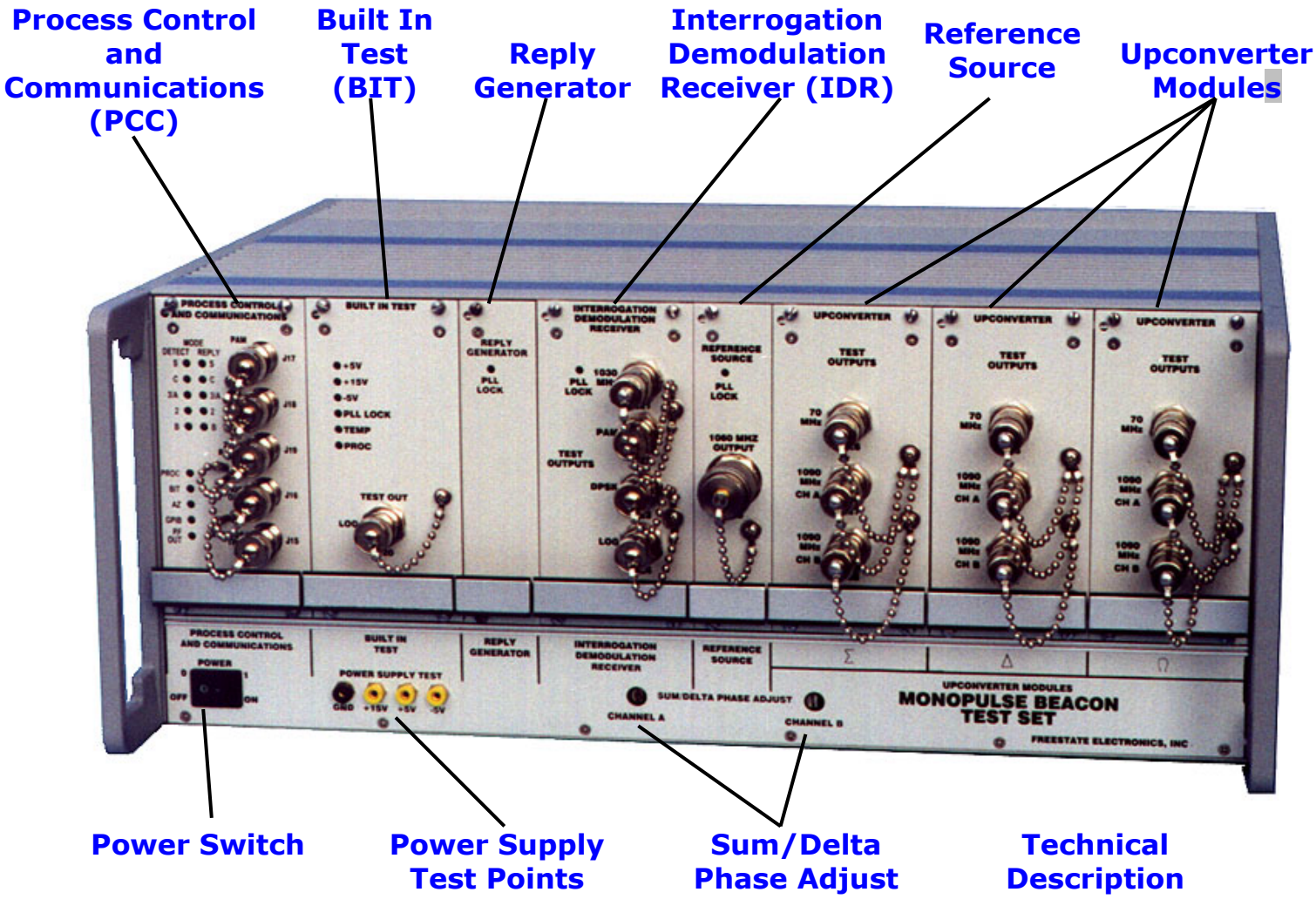
The MBTS electronics are contained within a 7" high by 19" wide chassis configured to mount into any standard equipment rack. All signal processing and generation takes place within eight plug-in modules. Included are one Reply Generator Module, three Upconverter Modules, one Interrogation Demodulator Receiver Module, one Reference Source Module, one Built In Test Module, and one Process Control and Communications Module. Each module uses blind-mate style connectors that attach to a mating connector on a motherboard assembly. This configuration simplifies the removal of any module for test or repair purposes, and also satisfies system maintenance and MTTR design requirements. The MTTR of any module is under five minutes. All modules are completely shielded to minimize EMI and RFI effects. Detailed chassis and module descriptions are found in Section 3.

1.3.2.1 MBTS Front Panel Overview

Figure 2 shows the modular structure of the MBTS mechanical design. The chassis design is based upon concepts inherent in the industry standard VXI chassis. However, because of rigorous RF signal specification requirements (phase, amplitude, and isolation) the mechanical design varies somewhat from VXI standards.

The eight plug-in modules are easily discerned. In addition to the plug-in modules, the chassis houses two power supplies, two RF phase adjusters (one for each Delta output channel), and a cooling fan. These items are permanently attached to the chassis. Power supply monitoring test points are located on the chassis front panel. Handles protect the front and rear panels from damage.

Figure 2. MBTS Front Panel

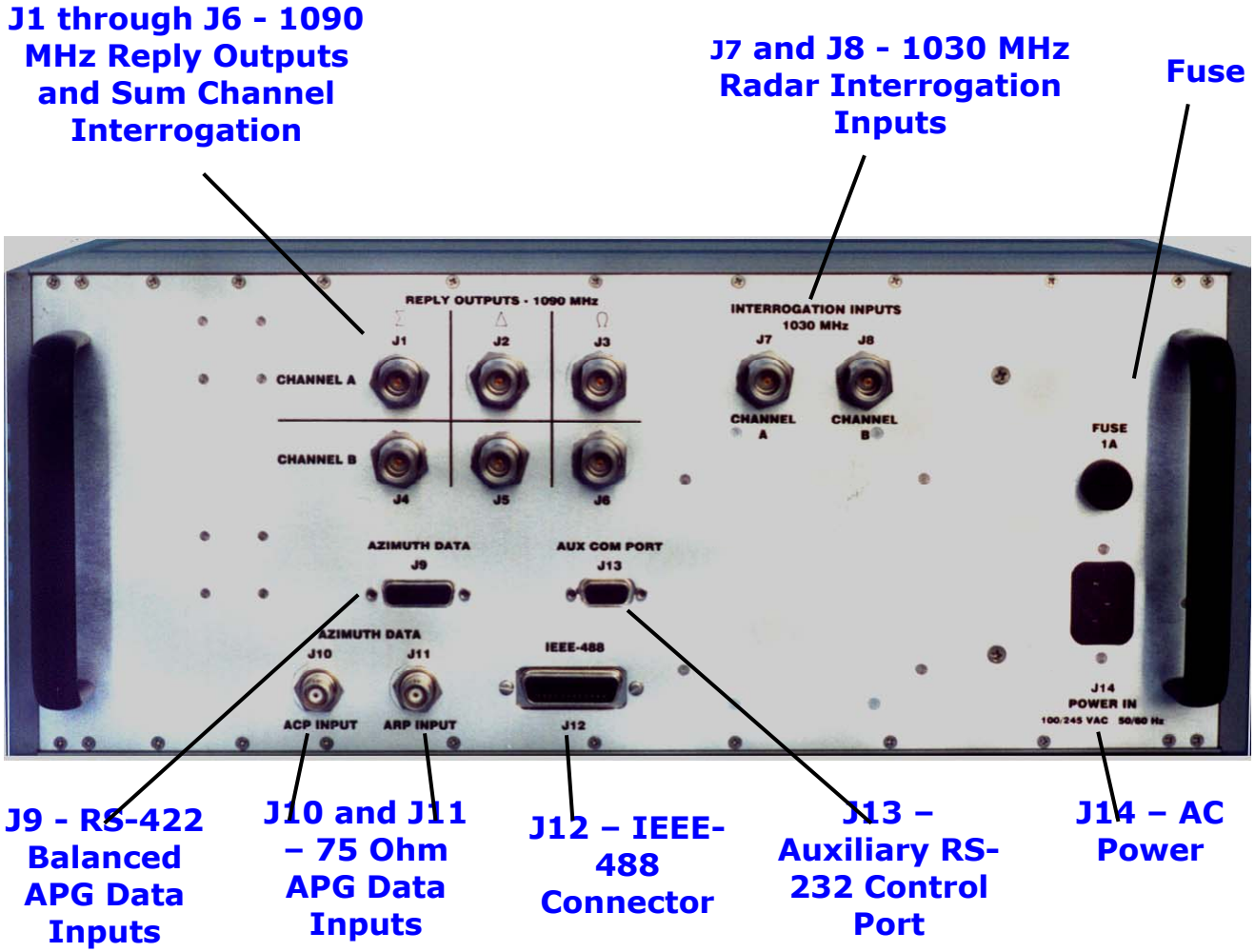


1.3.2.2 MBTS Rear Panel Overview

Figure 3 shows the rear panel of the MBTS. The rear panel includes various RF and data interfaces, the AC power input connector, and the fuse holder. Interrogation signals from a MSSR system are applied to the dedicated Interrogation Inputs, J7 or J8, or to the bi-directional Sum Channel ports, J1 or J4. MBTS reply signals are routed back into the MSSR receiver through either the Channel A (J1, J2, and J3) or Channel B (J4, J5, and J6) Sum, Delta, and Omni signal ports. Detailed descriptions of the use and function of each interface can be found by using the blue text links.

AC power is applied through an industry standard IEC filtered power connector located on the chassis rear panel. The MBTS operates from 115 to 230 VAC, at 50 - 60 Hz. The specified operational temperature range is from +10ºC to +50ºC.

Figure 3. MBTS Rear Panel

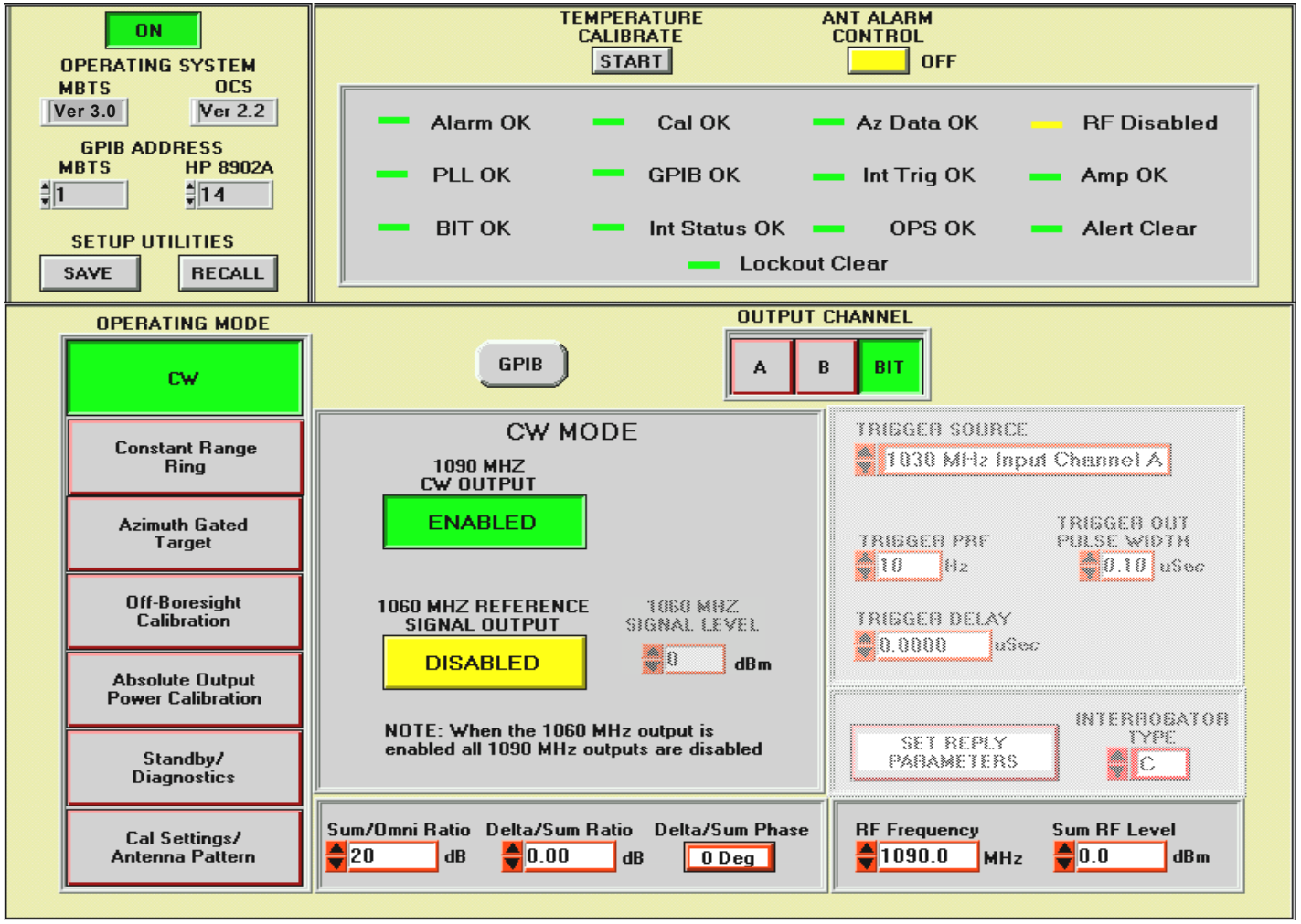


1.4 Operator Control Subsystem (OCS)

The MBTS Operator Control Subsystem (OCS) provides a straightforward means to control and monitor the operation of the MBTS unit. The OCS consists of a Pentium laptop computer configured with an IEEE-488 PCMCIA interface adapter and LabVIEW® based virtual instrument control software. Communication between the OCS and the MBTS unit is through the IEEE-488 interface. The MBTS IEEE-488 Command Set, FSE Document No. 100606, lists the commands, responses, and data formats required for proper remote control of the MBTS unit.

As shown in Figure 4, The OCS software creates a simulated MBTS instrument control panel from which all of the functions of the MBTS unit can be controlled. A menu bar allows the operator to choose from seven different MBTS operational modes: the CW Mode, the Constant Range Ring Mode, the Azimuth Gated Target Mode, the Off-Boresight Calibration Mode, the Absolute Output Power Calibration Mode, the Standby/Diagnostics Mode, and the Load Calibrated Antenna Pattern Mode. A selected set of operational conditions and target reply parameters are controlled in each mode of operation. All changes to control settings are automatically communicated to the MBTS. A detailed description of OCS functions, and of the various modes of MBTS operation, can be found in the OCS Screen Layout sections of the following chapter.

Figure 4. Typical OCS Control Panel



2 SYSTEM OPERATION

The MBTS system includes two primary components, the Monopulse Beacon Test Set (MBTS) and the Operator Control Subsystem (OCS). The OCS computer uses a Microsoft Windows® operating system. The OCS software is fully compliant with the Windows® system requirements. The following discussions assume a familiarity with the Windows operating system.

In addition to the MBTS System components, an HP-8902A Measuring Receiver with an 11722A Sensor is required for the periodic maintenance and calibration of the MBTS system.

2.1 Startup and Shutdown

2.1.1 System Startup

CAUTION

Always check the system configuration before making signal connections. The application of high-energy RF signals to inappropriate I/O connectors may damage the MBTS unit.

Use the following checklist when starting the system:

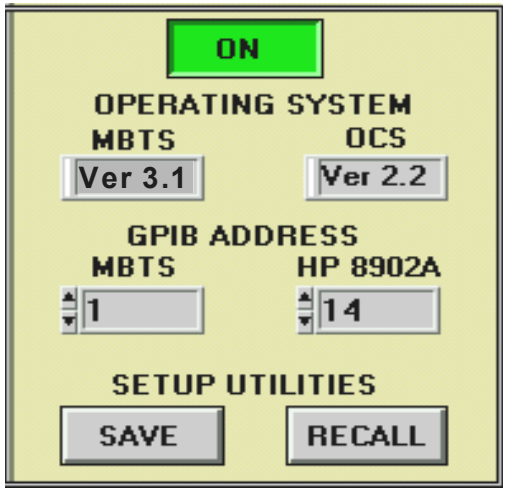
1. Verify the required operating configuration. If the MBTS is to be connected to a MSSR radar system carefully plan cable runs and connections before the application of signals. CAUTION: The application of high-energy RF signals to inappropriate I/O connectors may damage the unit. Refer to Section 6.1 of this manual for additional installation information.

2. Verify that the laptop computer is connected to the MBTS through the GPIB (IEEE-488) control port. The IEEE-488 adapter plugs into the laptop computer's PCMCIA slot.
3. Verify that the MBTS and the laptop computer are properly connected to a 110/220 VAC, 50/60 Hz power source.
4. Apply power to the MBTS. The Phase Locked Loop (PLL) indicators should illuminate GREEN on the Built In Test Module, the Reply Generator Module, the IDR Module, and the Reference Source Module. Upon completion of all Built-In-Test (BIT) diagnostic tests the PROC LED on the PCC Module front panel will flash on (green) and off once every second. In a quiet environment, the chassis fan should be heard running.
5. Apply power to the OCS computer. After Windows is fully loaded, activate the OCS software by double clicking on the "OCS" icon.
6. The OCS will automatically verify the GPIB connection to the MBTS and will load default operational parameters. By default, the OCS places the MBTS into the Azimuth Gated Target operating mode. When the Azimuth Gated Target mode control turns green the OCS virtual instrument panel is active and ready for operator input.

2.1.2 GPIB Address Setup

The GPIB bus addresses of the MBTS and of the external calibration equipment (HP-8902A) must agree with the addresses shown in the upper left area of the OCS window, as illustrated below. The addresses can be entered directly into the boxes, or they can be set to 0 through 31 by the use of the UP/DOWN arrows at the sides of the boxes. The MBTS is delivered from the factory set to GPIB address 1. The HP-8902A is typically set to address 14. More information on setting the MBTS hardware address is available in Section 3.2.6.2.1, PCC IEEE-488 Address Configuration and Calibration Setup.

Figure 5. OCS Shutdown Switch and IEEE-488 Address Select



2.1.3 MBTS Setup Save/Recall Functions

The operational settings of the MBTS may be saved to and recalled from a file using these controls.

To save the current operating parameters to a file click on the "SAVE" control. Either enter a name for the file to be created or select any file from the list displayed (it is not recommended to save to other than the default folder). Click on the "SAVE" control. After the file is saved the OCS will resume normal operation.

NOTE

Reply Code parameters are not saved by this function.

To recall a previously saved setup click on the "RECALL" control. Pick the desired file from the displayed list. The OCS will recall all saved operational parameters, load these into the MBTS, and reset the OCS control panel settings. By default, the OCS and MBTS are always set to the Azimuth Gated Target Mode after the use of the RECALL function.

2.1.4 Shutdown

Use the following procedure to properly shut down the system:

1. Close the OCS control panel by clicking the graphical ON Switch in the upper left menu area shown in Figure 5, above.

Note

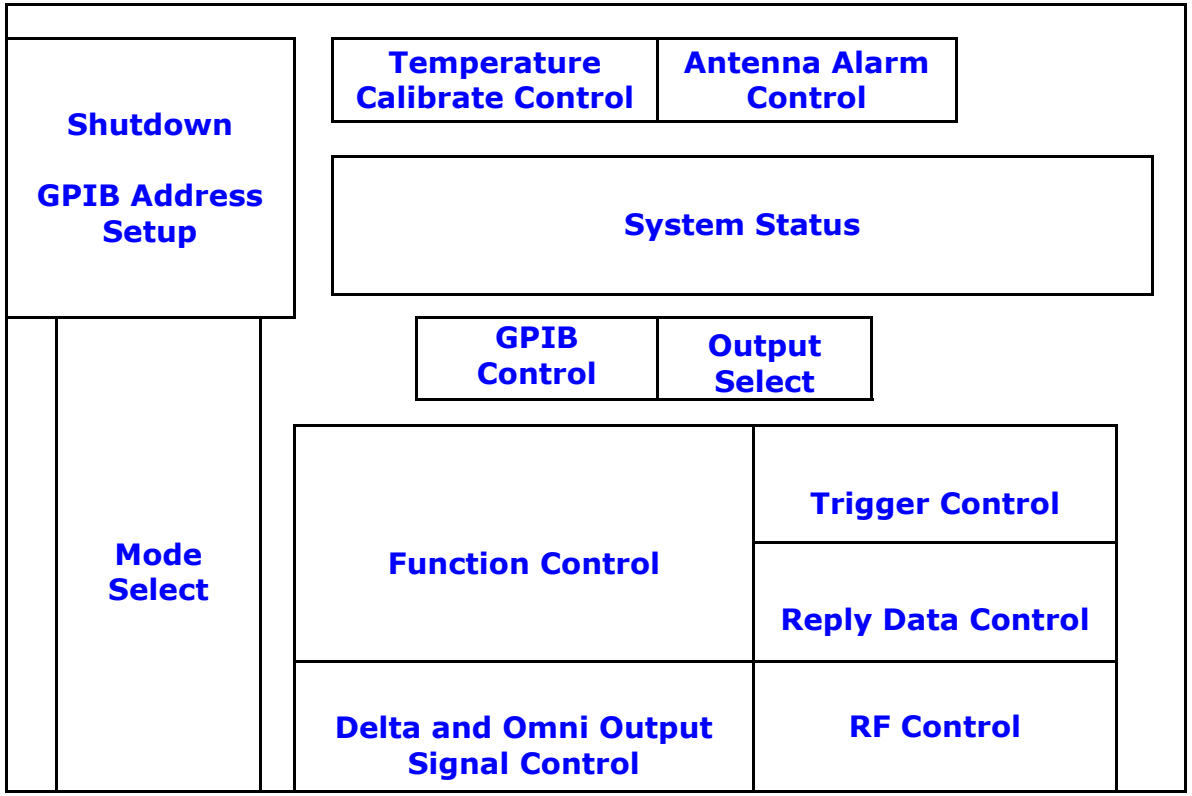
GPIB bus timeout errors will be generated if the MBTS is turned off before the OCS software is disabled.

2. After the OCS software has closed, and the Windows desktop is displayed, select SHUTDOWN from the Windows "START" menu located in the lower left corner of the computer screen.
3. Set the POWER switch on the front of the MBTS to the OFF position.

2.2 OCS Screen Layout

The OCS operating screen is a non-resizable window displayed on the Windows® operating system desktop. It consists of numerous controls and displays organized in the functional groups shown below. A description of each functional group may be found through the clicking on any of the light blue text links.

Figure 6. OCS Screen Layout



2.2.1 System Status

The System Status panel (see Figure 7) displays the status of important MBTS operating conditions and functions. The OCS monitors these on a continuous basis. Four colors are used to display function status.

Green indicates that the function is operationally active and working properly.

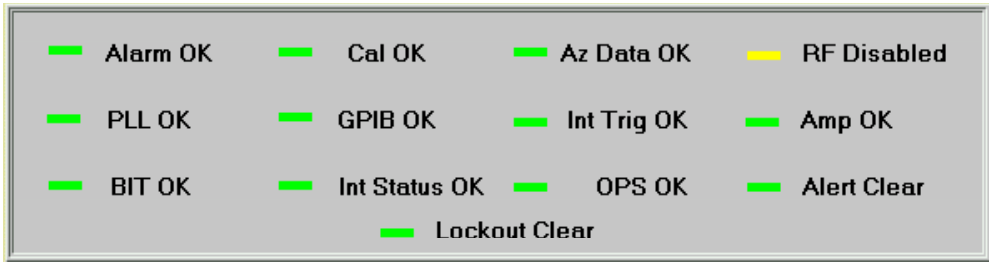
Yellow is a cautionary indicator. The function is either inactive or in an indeterminate state.

Red indicates that the function is in a failure mode. Critical function failures detected by the OCS force the MBTS into STANDBY Mode. Normal MBTS operations can resume only after the fault is corrected.

Blue indicates signal activity or a state that varies from default conditions. Lockout and Alert conditions, for instance, are indicated by this color.

The status of all monitored functions and operational conditions is displayed through the selection of the Standby/Diagnostics Mode. See Sections 2.3.6.4, and 5.2 for corrective actions in case of a failure.

Figure 7. System Status Display



2.2.1.1 Alarm Status Indicator

The Alarm Status Indicator displays the condition of the ALARM status register of the MBTS. Functions monitored include fan status, output signal calibration process, internal temperature, and power supply voltages. A fault condition for any of these functions results in a red indicator and an "Alarm Error" message.

2.2.1.2 Phase Lock (PLL) Indicator

The Phase Lock Indicator displays the status of the PLL status register of the MBTS. The condition of all MBTS phase locked loop circuits is monitored. Any detected fault condition results in a red indicator and a "PLL Error" message.

To OCS Screen Layout

2.2.1.3 BIT Status Indicator

The BIT Status Indicator displays the condition of that portion of INTERR status register of the MBTS related to BIT RF circuit test results. All RF control circuits are monitored. Any detected fault condition results in a red indicator and a "BIT Error" message.

2.2.1.4 Calibration Indicator

The Calibration Indicator changes to yellow and displays a "Cal Output" message whenever an internal recalibration of the MBTS output signal level is recommended. Recalibration is recommended when the internal temperature of the MBTS has changed significantly since the last calibration. When calibration of the MBTS is indicated, use the Temperature Calibrate control to adjust the output level of the MBTS.

2.2.1.5 GPIB Status Indicator

The GPIB Status Indicator displays the status of the GPIB link to the MBTS. Any detected fault condition results in a red indicator and a "GPIB Error" message.

2.2.1.6 Internal Status Indicator

The Internal Status Indicator displays the status of that portion of INTERR status register of the MBTS related to processor or memory function. Any detected fault condition results in a red indicator and a "Int Status Error" message.

2.2.1.7 RF Output Indicator

The RF Output Indicator is yellow whenever the output signal from the MBTS is disabled. It is green when the use of either Channel A or Channel B is selected.

2.2.1.8 Azimuth Status Indicator

The Azimuth Status Indicator is red, and a "Az Error" message is displayed, if data errors are detected from the azimuth pulse generator. Errors include lack of ARP or ACP data, improper ACP/ARP ratios, and improper rotation rates (high or low).

2.2.1.9 OPS Status Indicator

The OPS Status Indicator displays the status of the OP status register of the MBTS. It is yellow, and a "OPS Suspend" message is displayed, if MBTS operations are stopped or suspended. Changing target parameters, especially in Azimuth Gated Target Mode, may cause the generation of target replies to be temporarily suspended.

2.2.1.10 AMP Setting Status Indicator

The AMP setting Status Indicator is yellow, and a "AMP Conflict" message is displayed, if the settings of the Sum Output power, Delta/Sum ratio, or Sum/Omni ratio controls exceed the capabilities of the MBTS. Achieved signal levels from the Sum, Delta, and Omni outputs will not be as indicated by control settings.

2.2.1.11 ALERT Activity Indicator

The ALERT Activity Indicator is blue and displays an "ALERT Active" message whenever the MBTS is set to generate replies with the Alert bit set. The Alert signal is generated in response to changes to the Mode 3/A code setting.

2.2.1.12 LOCKOUT Activity Indicator

The LOCKOUT Activity Indicator is blue and displays a "LOCKOUT Active" message whenever any reply Lockout condition is set in the MBTS. The Lockout condition is set in response to data commands received from radar system Roll-Call interrogations.

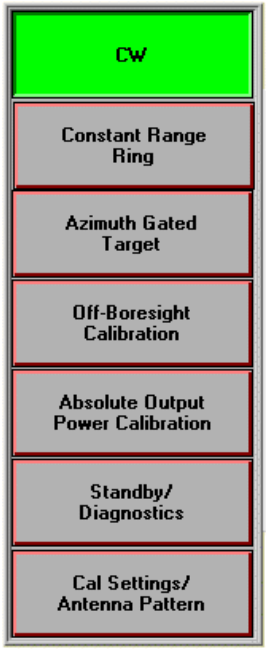
2.2.1.13 TRIG Status Indicator

The TRIG Status Indicator is yellow, and a "TRIG Conflict" message is displayed, if the settings of the internal trigger rate control and the range control are incompatible. Reply signals will not be generated at the rate indicated by the control settings. Trigger status is only checked when internal triggers are used to generate reply signals.

2.2.2 Mode Select

The setting of the Mode Select control determines the operating mode of the MBTS. The selected mode is highlighted as shown in the illustration below. Operating parameters and controls pertinent to the selected mode of operation are displayed in the Function Control area. A complete description of each operating mode can be found within the MBTS Operational Mode Selection section.

Figure 8. Mode Select Panel

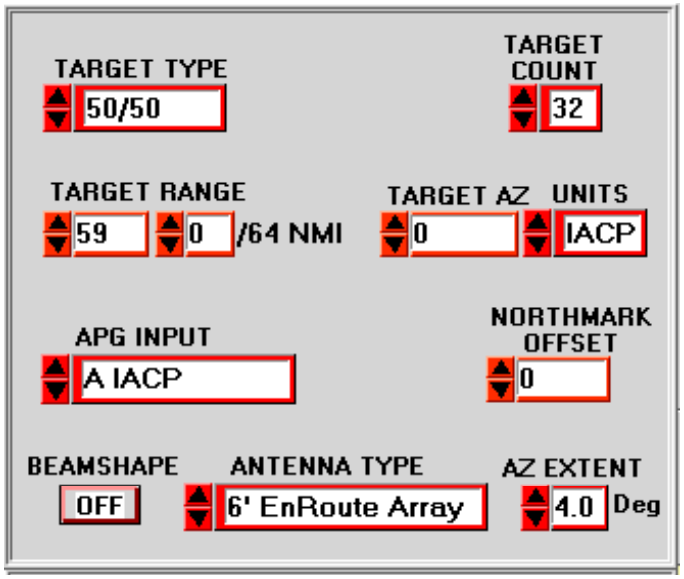


To OCS Screen Layout

2.2.3 Function Control

The displayed Function Control panel is specific to the selected operating mode (refer to the Mode Select options). Figure 9, for instance, illustrates the Function Control Panel displayed when operating in the Azimuth Gated Target Mode. Detailed descriptions and information about the use of each type of Function Control Panel is included in the MBTS Operational Modes section.

Figure 9. Typical Function Control Panel

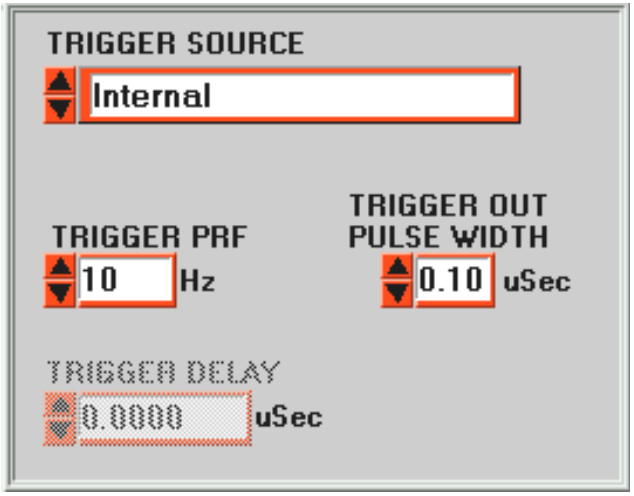


To OCS Screen Layout

2.2.4 Trigger Control

A trigger signal is required by the MBTS to generate pulsed RF target replies. The Trigger Control panel allows the selection of a number of trigger signal sources, including RF interrogations, Mode Pair signals, and internal or external pulse signals. Additional trigger controls are made available dependent upon the trigger source selected. These include, Trigger Pulse Repetition Frequency (PRF), Trigger Pulse Width, and Trigger Delay. The use of each trigger control is described in detail in the following paragraphs.

Figure 10. Trigger Control Panel

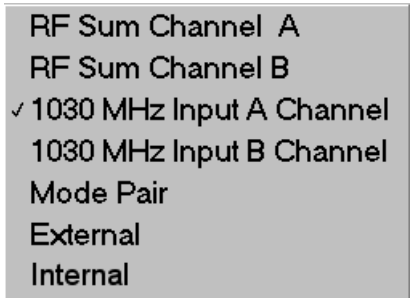


2.2.4.1 Trigger Source

As seen in Figure 11, selectable trigger sources include RF interrogations, Mode Pair pulses, and internal or external pulses. RF interrogations can be routed into the MBTS through four signal paths. These include the Sum Channel A or B connections (J1 and J4) or the 1030 MHz Channel A or B Interrogation Inputs (J7 and J8). See Figure 3, MBTS Rear Panel, for connector locations. ATCRBS Mode Pair or external trigger pulses are applied to the EXT/MODE Trigger connector located on the front panel of the PCC Module (see PCC Module Front Panel Connectors). A free running pulse generator, internal to the PCC Module, may also be selected as the trigger source.

Trigger signals derived from either demodulated interrogations, or from ATCRBS Mode Pair signals, are decoded, processed, and formatted to generate the proper target reply signal. Use of external trigger signals, or the selection of internal triggering, requires the selection of an Interrogator Type in the Reply Control panel.

Figure 11. Trigger Source Selection Window



Trigger source selections are made using the up/down arrows, or by clicking on the Trigger Source display area, and then choosing a trigger source from the displayed options.

The following paragraphs provide more detail on the various trigger options.

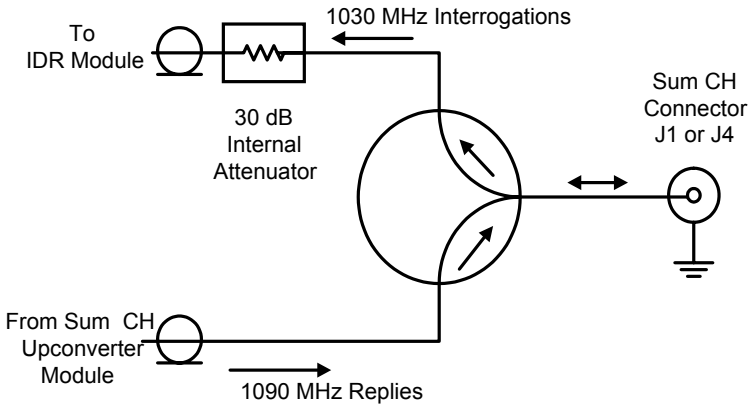
NOTE

The time between consecutive trigger signals must be greater than the time it takes for the MBTS to generate a reply response. Make sure that the Range setting of the MBTS is appropriate for the repetition rate of the applied trigger signal. When the Internal trigger option is selected a Trigger Conflict message will appear in the Status window if the Range and Trigger PRF settings are incompatible.

RF Sum Channel Interrogation Triggers. Some radar systems, such as the ATCBI-6, diplex the 1030 MHz interrogation and the 1090 MHz reply signals onto a single RF cable. The MBTS supports this operational configuration. Two microwave circulators, internal to the MBTS, route the interrogation and reply signals to their proper destinations (see Figure 12, below). Triggering the MBTS in this case is accomplished by selecting the RF Sum Channel input for either Channel A or Channel B. Signal connections with the MBTS are through either J1 (Sum Channel A), or J4 (Sum Channel B). Both of these are located on the MBTS Rear Panel. Delta and Omni channel system cabling requirements are unaffected by the use of the Sum Channel triggers. Because the Sum Channel interrogation signals are at a substantially higher signal level, up to 50 Watts peak, than those that are applied to the MBTS through the

dedicated interrogation input channels, the configuration of the system should be thoroughly verified prior to the application of power.

Figure 12. SUM Channel Circulator Signal Flow



1030 MHz Input Interrogation Triggers. The MBTS has two dedicated interrogation (only) signal input connections. The Channel A (J7) and Channel B (J8) interrogation inputs are located on the MBTS Rear Panel. To trigger from interrogation signals on these ports choose either the 1030 MHz Input Channel A selection or the 1030 MHz Input Channel B selection, as appropriate.

Mode Pair Triggers. ATCRBS Mode Pair pulse sequences can be used to trigger replies from the MBTS. In this case, the Mode Pair video signal is applied to the MBTS through J15 – Mode/External Trigger, located on the front panel of the Process Control and Communications (PCC) Module (see Figure 53 for connector location).

External Pulse Triggers. TTL level pulse signals may be used to trigger replies from the MBTS. Pulse trigger signals are applied to the MBTS through (J15), located on the front panel of the Process Control and Communications (PCC) Module. The repetition rate of the applied pulse triggers must be between 1 and 3,000 pulses per second. When external pulses trigger MBTS replies the setting of the Interrogator Type control (see the Reply Data Control panel) determines the type of reply response. Note: The value of the associated Trigger Delay control must always be less than the time between trigger pulses.

Internal Pulse Triggers. Internally generated pulses may be used to trigger repetitive replies from the MBTS. Trigger rate and pulse width are set through the use of the Trigger PRF and Trigger Pulse Width controls as described in the next two sections. Trigger characteristics may be monitored at the Trigger Output (J16) of the MBTS located on the front panel of the Process Control and Communications (PCC) Module. When internal pulses trigger MBTS replies the setting of the Interrogator Type control (see the Reply Data Control panel) determines the type of reply response.

2.2.4.2 Trigger PRF

The PRF of internally generated triggers can be varied from 10 to 1,000 Hertz in 5 Hz increments. The PRF value may be set using either the UP/DOWN controls or by direct keyboard entry.

2.2.4.3 Trigger Pulse Width

The pulse width of the TTL signal at the Trigger Out connector (J16) can be varied from 0.1 to 5.0 microseconds in 0.1 microsecond increments. The Pulse Width setting is made through the use of either the UP/DOWN controls or by direct keyboard entry.

2.2.4.4 Trigger Delay

When external pulses are used trigger MBTS replies, a delay can be set between the application of the trigger pulse and the generation of a Trigger Out signal. The delay can be set to a value of from 0.0 to3.0 milliseconds in increments of 62.5 nanoseconds. The Trigger Delay value may be set using either the UP/DOWN controls or by direct keyboard entry. The timing of the reply signal is unaffected by this function.

2.2.5 Reply Data Control

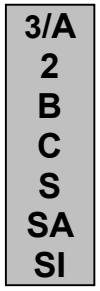
The Reply Data Control panel is used to set reply signal data content such as the interrogation type (when operating in External or Internal trigger modes), or reply code parameters. Controls are also available for varying reply pulse width and position parameters from nominal values.

Figure 13. Reply Control Panel

2.2.5.1 Interrogator Type

When the use of external or internal pulse triggers is selected, the Interrogator Type control assigns an interrogator type to the trigger signal. This assignment is required by the MBTS to determine the proper reply response. Interrogator type choices, as seen in Figure 14, include ATCRBS Type 2, B, C, and 3/A, Mode S All-Call (S), Mode S Roll-Call Altitude (SA), or Mode S Roll-Call ID (SI). The Interrogator Type setting is disregarded when replies are triggered from either RF interrogations or Mode Pair signals.

Figure 14. Interrogator Type Selection Menu



2.2.5.2 Set Reply Parameters

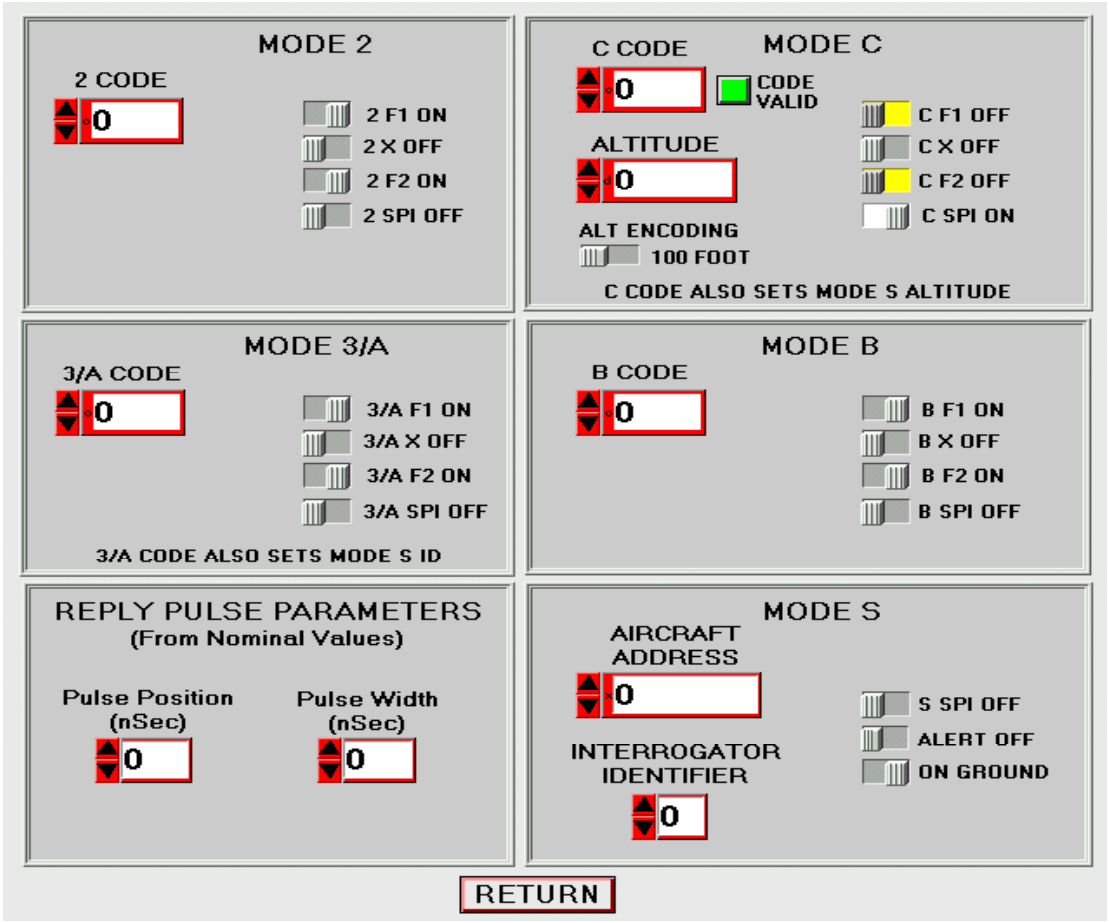
Activating the SET REPLY PARAMETERS control opens the REPLY PARAMETERS window as seen in Figure 15. The controls within this window set all user variable code and pulse parameters for each reply type.

ATCRBS Reply Parameters. The upper four control panels within the Reply Parameter window are used to independently set the reply code parameters of each of the four possible ATCRBS reply types (2, B, C, and 3/A). Reply code values may be set from 0000 to 7777 (octal). Additional controls allow the operator to set or delete the F1, F2, X and SPI pulses from the reply sequence.

The Mode C panel allows direct entry of aircraft altitude in feet or a C code value. The C code and altitude controls are interactive; entries in one automatically update the other. C code values that do not map to an altitude result in a "Code Invalid" message. In this case the Mode S altitude is set to -1000 ft. An altitude-encoding switch sets encoding resolution to either 100 feet or 25 feet. When altitude encoding is set to 25 feet, C code entry is disabled. Mode S Roll-Call altitude reply data, in response to a Mode-S altitude interrogation (UF=4), is determined from the indicated Altitude setting.

The Mode 3/A panel allows direct entry of transponder ID codes. This code value also sets the MBTS response to Mode S Roll-Call ID (UF=5) interrogations. Changing the 3/A code temporarily sets the Alert bit in MBTS generated Mode S replies. The Alert bit is active for 18 seconds after a change in code value is entered into the MBTS.

Figure 15. Reply Parameter Window



To OCS Screen Layout

Pulse Parameters. This panel contains controls that set the pulse width and spacing parameters of the pulsed RF reply signals. Both parameters may be varied +/- 250 nanoseconds from nominal settings in 50 nanosecond increments. Mode S data pulses are not altered by these control settings.

MODE S Reply Parameters. This panel contains controls to set the Mode S Aircraft Address and Mode S Interrogator ID parameters. The Aircraft Address value may be set from 000000 to FFFFFF (hex). When operating in Azimuth Gated Target Mode the Aircraft Address value is applied to the first target after the ARP pulse (with the Northmark offset control set to a value of 0). The address value of subsequent Mode S targets increment from the displayed control setting.

NOTE

The Northmark offset control can rotate the azimuth position of the target constellation such that the "first target" location is not the first encountered after the ARP pulse.

The Interrogator ID value may be set from 0 to 63. The selected Interrogator ID value is used to formulate the encoded reply data sequence when the MBTS is triggered from external or internal pulses. When Mode S replies are triggered from RF interrogation triggers the interrogator ID value is derived from the demodulated interrogation data.

Also included in the Mode S parameters field are controls for setting the Mode S SPI bit, for setting a permanent Mode S Alert bit, and for setting the Mode S aircraft flight status (Airborne/On Ground) bit. Unlike the timed (18 second) Alert signals triggered by a change in aircraft ID, the Mode S Alert control will permanently set the Alert bit in Mode S replies until the state of the control is changed.

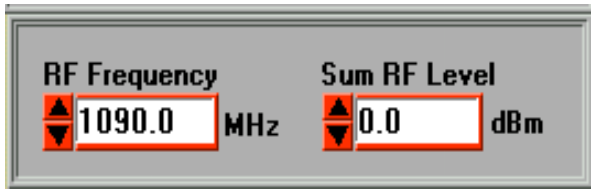
2.2.6 RF Control

The controls within the RF Control panel set the frequency and level of the Sum Channel output of the MBTS. The Delta and Omni output signal levels are always relative to the indicated Sum level setting. The RF Frequency setting applies to the Sum, Delta, and Omni outputs.

NOTE

The Sum RF level is also often referred to as the "target" signal level.

Figure 16. RF Control Panel



2.2.6.1 RF Frequency

The RF Frequency control sets the frequency of the Sum, Delta, and Omni outputs. The frequency can be set from 1080.0 to 1100.0 MHz, in 0.2 MHz steps.

2.2.6.2 Sum RF Level

The Sum RF Level control sets the output level of the Sum Channel signal. The adjustment range of the Sum RF Level control is from –85 to +10 dBm in 0.5 dB increments. The indicated level applies to signals at the selected Rear Panel Sum Channel output, Channel A (J1) or Channel B (J4). Changes to the control setting also change the output level of signals at the MBTS Upconverter Module 1090 MHz and 70 MHz test ports.

Front Panel 1090 MHz Outputs. The level of signals at the Upconverter Module 1090 MHz test output ports are approximately 20 dB below the level of signals at the rear panel outputs.

Front Panel 70 MHz Output. The level of signals at the Upconverter Module 70 MHz test output ports are approximately 15 dB below the level of signals at the rear panel outputs.

NOTE

The amplitude level of the DELTA and OMNI RF outputs are set relative to the SUM RF Level. Thus, changing the SUM output level also changes the level of the DELTA and OMNI outputs.

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2.2.7 Delta and Omni Output Signal Controls

The controls within this panel set the output level of the Delta and Omni Channel signals. The indicated output levels are relative to the Sum Channel, or "target", output level. An additional control sets the Delta Channel to Sum Channel phase relationship. In some modes of operation one or more of these signal parameters are set automatically. In these cases the use of the affected control will be disabled (grayed out).

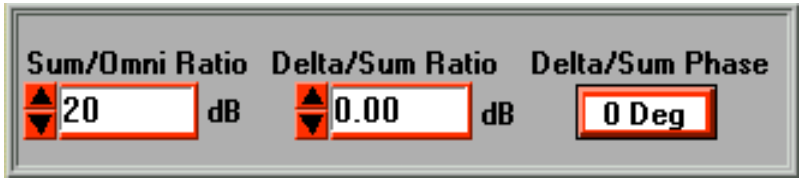


Figure 17. Monopulse Antenna Control Panel

Data entries can be made using the UP-DOWN buttons, or through keyboard entry.

2.2.7.1 Delta-to-Sum Ratio

The Delta/Sum Ratio control sets the level of the Delta Channel signal relative to that of the Sum Channel signal. Signals at the MBTS Rear Panel Delta Channel A (J2), and Delta Channel B (J5) outputs are affected. The adjustment range of this control is from –41.75 to +12.0 dB, in 0.25 dB increments.

NOTE

The maximum Delta Channel output level is +16 dBm. The combination of Sum Channel output level and Delta/Sum ratio should not be set to exceed this level. Doing so will result in indeterminate signal levels. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

2.2.7.2 Sum-to-Omni Ratio

The Sum/Omni Ratio control sets the level of the Omni Channel signal relative to that of the Sum Channel signal. Signals at the MBTS Rear Panel Omni Channel A (J3), and Omni Channel B (J6) outputs are affected. The adjustment range of this control is from –28 to +20 dB in 1 dB increments.

NOTE

The maximum output level for the Omni Channel is -10 dBm. The combination of Sum Channel output level and Sum/Omni ratio should not be set to exceed this level. Doing so will result in indeterminate signal levels. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

2.2.7.3 Delta-to-Sum Phase

The Delta to Sum Phase Control sets the phase relationship between the rear panel Sum and Delta Channel signals. Available control settings are 0 degrees and 180 degrees.

The Sum/Delta phase relationship of either output channel can be trimmed to exact requirements through use of the phase adjustment screws found on the MBTS Front Panel. Sum/Delta phase relationships are not guaranteed at front panel test ports.

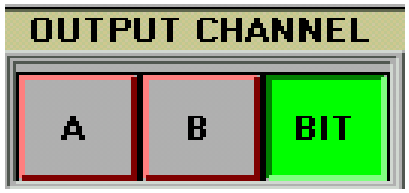
2.2.8 Output Select

The Output Select control sets the RF signal path through the MBTS. Control options include the selection of output Channel A, output Channel B, or BIT (Built-In Test). The Channel A and B settings route signals to either the Channel A or the Channel B Sum, Delta, and Omni output connectors located on the Rear Panel of the MBTS. The control setting also determines signal presence at the 1090 MHz Channel A and Channel B test ports located on the front panel of each Upconverter Module.

The BIT setting routes the 1090 MHz signal of each Upconverter Module to the BIT Module. This signal path is automatically chosen whenever the operational mode of the MBTS is changed. The MBTS initializes with the BIT path selected.

The selected signal path is highlighted in bright green, as shown below.

Figure 18. Output Select



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2.2.9 GPIB Control

The GPIB control opens a GPIB control window (as seen in Figure 19), and a new GPIB session, in which any of the operational parameters of the MBTS may be set and monitored through the entry of an appropriate GPIB command. This control provides a convenient means of controlling and verifying MBTS operations independent of OCS operations.

Commands are entered into the Command text box and sent to the MBTS by use of the READ control. Command responses are displayed in the Response text area. The MBTS IEEE-488 Command Set document, FSE document number 100606, lists and describes the use of all applicable commands. Clicking on the QUIT control closes the GPIB window, and transfers control of MBTS processes back to the OCS.

The GPIB control should be used with caution since the OCS cannot track changes made to the operational state of the MBTS through its use. This means that, upon returning to normal OCS control, the OCS may display incorrect MBTS operating conditions. All OCS operations are suspended while the GPIB command session is open.

Figure 19. GPIB Control Window

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2.2.10 Antenna Alarm Control

The Antenna Alarm control enables and disables the monitoring of data from the selected Azimuth Pulse Generator (APG) source. When the antenna alarm function is enabled the azimuth reference pulse (ARP) and azimuth change pulse (ACP) data at the selected MBTS input is checked for signal presence, timing, pulse count, data type (ACP or IACP), and antenna rotation rate. Out of specification conditions trigger the antenna alarm. APG input signal specifications are listed in Sections 4.2.1.3, J9 - RS-422 Balanced APG Data Inputs, and 4.2.1.4, J10 and J11 – 75 Ohm APG Data Inputs, of this manual.

The alarm condition is indicated by a red AZ LED on the front panel of the PCC Module of the MBTS and by an "Az Error" message in the System Status window on the OCS display. The MBTS will not generate target replies when an azimuth alarm condition is present. The MBTS AZ alarm is cleared by applying compliant APG signals to the selected MBTS input or by disabling the antenna alarm function. The antenna alarm function should be disabled whenever there is no APG source or if MBTS operation with manually stepped azimuth data is required.

Compliant APG data must be available to the MBTS to enable operation in the Azimuth Gated Target Mode. Other MBTS modes of operation do not need APG signals. In these cases the antenna alarm function can be disabled. The APG Input control, found in the Function Control panel, is used to select the rear panel connection and type of APG data processed by the MBTS. Azimuth signals may be applied to connectors J9, J10, and J11 on the Rear Panel of the MBTS.

Figure 20. Antenna Alarm Control and Temperature Calibrate Control

To alert the operator to non-compliant APG operating conditions an "Az Error" is displayed in the System Status window (see Figure 7).

2.2.11 Temperature Calibrate Control

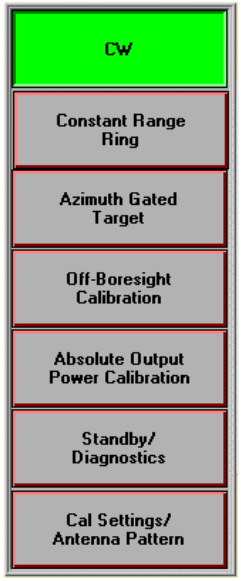
The Calibration Indicator on the OCS System Status Display turns yellow when a significant change in the operational temperature of the MBTS is detected. This indicates the need to adjust the output level of the MBTS. Clicking on the Temperature Calibrate control adjusts the amplitude characteristics of the MBTS. If the calibration process is successful, the Calibration Indicator will turn from yellow to green. The Temperature Calibrate control may also be used to minimize any changes in output amplitude that arise from changing the operating frequency.

To OCS Screen Layout

2.3 MBTS Operational Modes

The illustration below indicates the seven operational modes of the MBTS and the OCS controls used to select them. A complete description of any operating mode may be found by clicking on the appropriate text link below.

Figure 21. MBTS Operational Mode Selection



CW Mode

Constant Range Ring Mode

Azimuth Gated Target Mode

Off-Boresight Calibration Mode

Absolute Output Power Calibration Mode

Standby/Diagnostics Mode

Cal Settings/Antenna Patterns Mode

2.3.1 CW Mode

When in the CW mode the MBTS generates CW RF signals at the selected output(s). The operator may designate the MBTS to operate in either the 1090 MHz CW Mode or in the 1060 MHz CW Mode. 1090 MHz operation is the default condition.

When in the 1090 MHz CW Mode the MBTS creates CW signals that are available at either set of Sum, Delta, and Omni output channels located at the rear panel of the MBTS. These signals may then be used in a variety of ways to verify radar system performance.

When in the 1060 MHz CW Mode the MBTS generates a 1060 MHz test signal at the front panel 1060 MHz RF output (J25) of the Reference Source Module. This signal may be used as an aid in the calibration and alignment of the MSSR antenna.

Detailed information concerning each mode of CW operation is available by selecting one of the two text links above.

To MBTS Operational Mode Selection

2.3.1.1 1060 MHz CW Mode

While operating in this mode the MBTS generates a 1060 MHz CW test signal at J25, located on the front panel of the Reference Source Module. When this mode is enabled no signals are available at any of the 1090 MHz MBTS output ports.

The 1060 MHz CW mode is entered by clicking on the 1060 MHz Reference Signal Output control located in the CW Mode Function Control panel (see Figure 22 below).

The output power level of the 1060 MHz signal is adjustable from -22 dBm to +8 dBm in 1dB increments. The Signal Level control sets the signal output power to the desired level. See Section 4.2.2.5, J25 – 1060 MHz Test Output, for detailed information on output signal specifications.

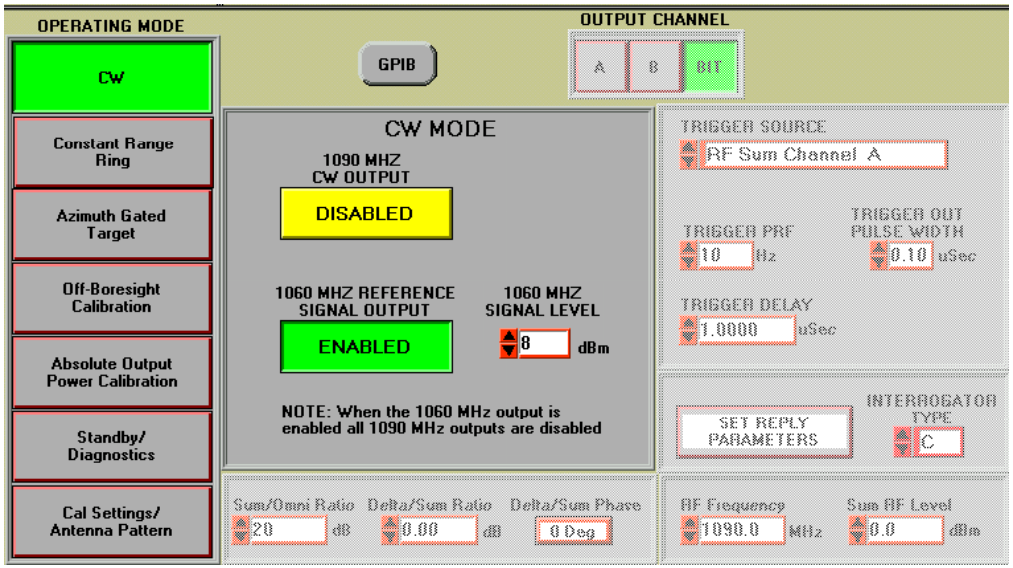


Figure 22.
1060 MHz CW Mode OCS Screen

2.3.1.2 1090 MHz CW Mode

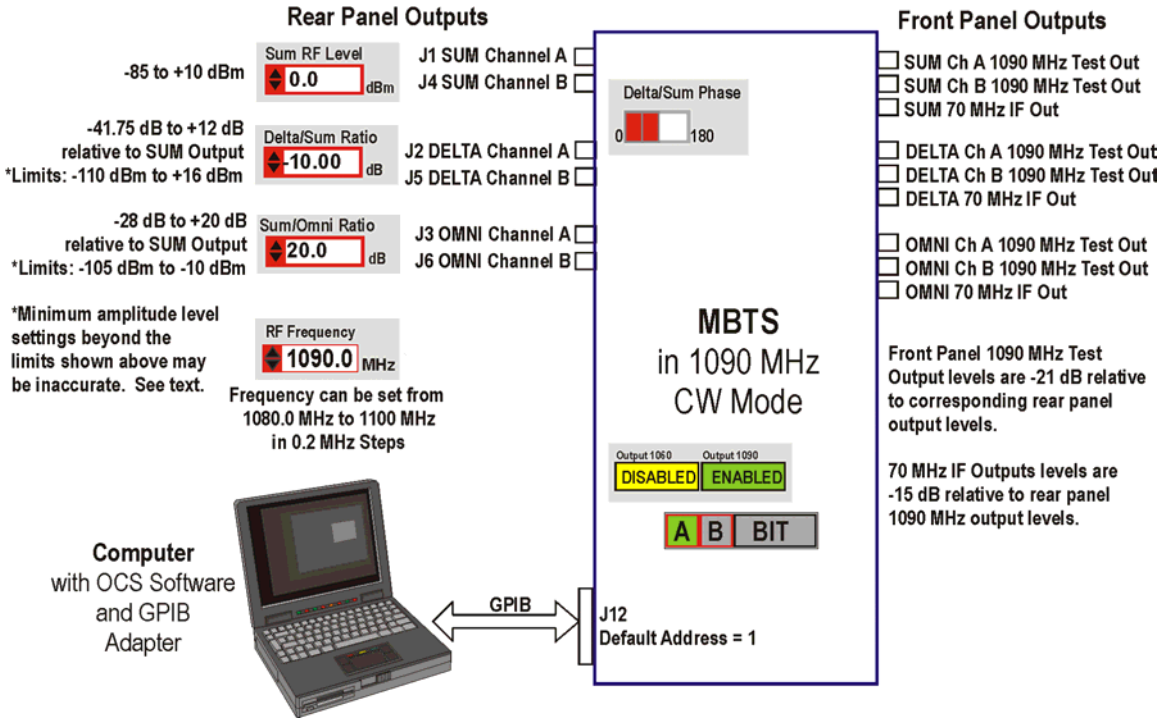
2.3.1.2.1 Overview

The 1090 MHz CW Mode configures the MBTS to generate signals suitable for analyzing CW characteristics of radar system performance, testing RF components or assemblies, and for verifying system interconnections of the MBTS to the radar system.

When in the 1090 MHz CW Mode the MBTS generates unmodulated RF signals. These frequency stable and amplitude accurate RF signals are found at the primary MBTS outputs, located on the chassis Rear Panel, as well as at test output ports, located on the chassis Front Panel at each of the three Upconverter Modules. The primary outputs consist of two channels, A and B, of SUM (Σ), DELTA (Δ), and OMNI (Ω) signals. Only one output channel is active at a time. Test signal ports include a 1090 MHz Channel A output, a 1090 MHz Channel B output, and a 70 MHz output for each of the Sum, Delta, and Omni signal paths.

Amplitude, frequency, phase, and output signal path controls are found on the 1090 MHz CW Mode OCS Screen control panel of the Operator Control Subsystem (OCS) . The 1090 MHz CW Mode Control Functions diagram, Figure 23, shows how the various OCS controls affect signal characteristics at each MBTS output. Use of these controls is described in the following sections.

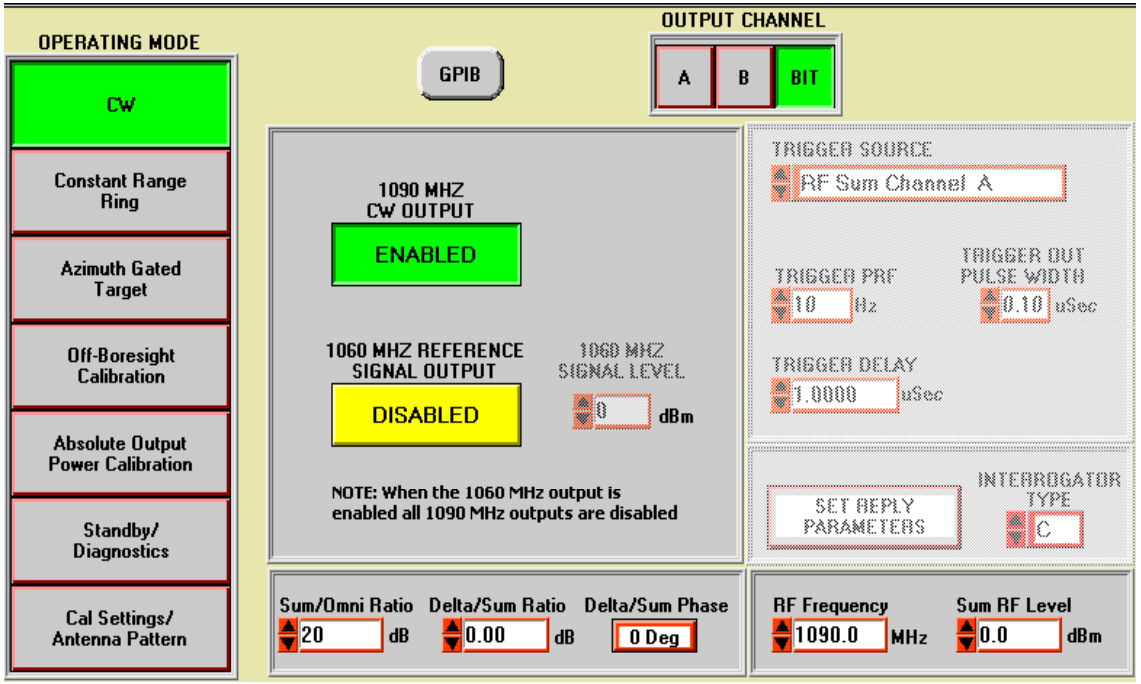
Figure 23. 1090 MHz CW Mode Control Functions



2.3.1.2.2 1090 MHz CW Mode Operation

To use the 1090 MHz CW mode, the MBTS and the OCS must be configured and activated as described in the System Startup section. Use the OCS Mode control to place the MBTS into the CW Mode. The CW Mode OCS control panel appears as shown in Figure 24. The 1090 MHz CW Mode is active when the 1090 MHz CW Output control is ENABLED.

Figure 24. 1090 MHz CW Mode OCS Screen



2.3.1.2.3 1090 MHz CW Mode Connections

CW signals are routed to the primary MBTS outputs, located on the chassis Rear Panel, as well as to test output ports, located on the chassis Front Panel at each of the three Upconverter Modules.

The MBTS has two primary outputs channels, A and B, each consisting of separate SUM (∑), DELTA (Δ), and OMNI (Ω) signals. The Channel A Sum, Delta, and Omni 1090 MHz output connectors are identified as J1, J2, and J3 respectively. The Channel B Sum, Delta, and Omni output connectors are identified as J4, J5, and J6 respectively. Only one output channel is active at a time. Output channel selection is made through the use of the Output Select control.

Front panel test signal ports include a 1090 MHz Channel A output (J27), a 1090 MHz Channel B output (J28), and a 70 MHz output (J26) for each of the Sum, Delta, and Omni signal paths. The Output Select control, mentioned above, also controls which of the two 1090 MHz test ports is active.

Front Panel 1090 MHz Outputs. Signals at the active 1090 MHz test output ports are approximately 20 dB below the level of signals at the corresponding rear panel outputs. For instance, if the rear panel SUM Channel A output signal is at a level of -10 dBm, the Sum Channel A 1090 MHz Test Output signal level will be approximately –30 dBm.

Front Panel 70 MHz Outputs. Signals at the 70 MHz test output ports are approximately 15 dB below the level of signals at the corresponding rear panel outputs. For instance, if the rear panel SUM Channel A output signal is at a level of 0 dBm, the SUM Channel 70 MHz Test Output signal level will be approximately –15 dBm.

2.3.1.2.4 1090 MHz CW Mode OCS Controls

The following OCS controls, as shown on the 1090 MHz CW Mode OCS Screen, are used to set the operational parameters of CW signals generated by the MBTS.

RF Frequency. The OCS RF Frequency panel sets the output frequency of all RF signals. The default operating frequency is 1090.0 MHz. Signal frequency can be adjusted from 1080.0 to 1100.0 MHz, in 0.2 MHz steps.

The frequency of all IF signals at the 70 MHz Upconverter Test ports is fixed at 70 MHz. The frequency of these signals does not vary due to frequency changes made to the RF outputs.

SUM Output Level. The Sum RF Level controls sets the output amplitude of the Channel A and Channel B SUM RF signals. Output signal level can be set to between –85 dBm and +10 dBm in 0.5 dB increments.

NOTE

The amplitude level of the DELTA and OMNI RF outputs are set relative to the SUM RF Level. Thus, changing the SUM output level also changes the level of the DELTA and OMNI outputs.

DELTA Output Level. The Delta-to-Sum Ratio control sets the level of the Delta Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –41.75 to +12.0 dB, in 0.25 dB increments.

NOTE

The operator should set the DELTA RF control so as to maintain DELTA RF signals at or between absolute amplitude levels of –110 dBm and +16 dBm. The OCS Delta/Sum control allows settings outside of this range. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

OMNI Output Level. The Sum-to-Omni Ratio control sets the level of the Omni Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –28 to +20 dB in 1 dB increments.

NOTE

The operator should set the OMNI RF control so as to maintain OMNI RF signals at or between absolute amplitude levels of –105 dBm and -10 dBm. The OCS Sum/Omni control allows settings outside of this range. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

DELTA Output Phase. The Delta-to-Sum Phase control sets the phase of the Delta signal channel relative to that of the Sum Channel signal. The control allows selection of either an in-phase state (zero degree) or a 180-degree phase state. Phase matching applies only to the Channel A and B Sum and Delta outputs located on the rear panel of the MBTS. The phase relationship of the 1090 MHz and 70 MHz test output signals is not guaranteed.

Output Channel Selection. Only one output channel, A or B, is active at a time. Output channel selection is made through the use of the Output Select control. RF Output System Status indicators, one on the PCC front panel and the other on the OCS status panel, are GREEN if either output Channel A or output Channel B is selected. If the BIT setting of the Output Select control is selected, both output status indicators will be YELLOW.

NOTE

If there appears to be a signal level problem with the MBTS, check the status of the Output Select control. Often no RF output channel has been selected.

2.3.2 Constant Range Ring Mode

When in the Constant Range Ring Mode the MBTS generates pulsed RF replies in response to all valid trigger signals. The amplitude of the Sum, Delta, and Omni pulsed reply signals is fixed at operator selectable settings. Reply generation is not gated by target position as it is in the Azimuth Gated Target Mode.

While in this mode the MBTS generates replies in response to ATCRBS or Mode S RF interrogations, ATCRBS mode pair triggers, internal triggers, and external triggers. The trigger signal input is selected through the use of the Trigger Source control. The Target Type control sets the MBTS to simulate an ATCRBS target, a Mode S target, or a 50/50 mix of both ATCRBS and Mode S targets. The Range control sets the timing of the MBTS reply to properly simulate a target at a range of from 0.5 to 255 nautical miles (nmi).

The pulsed RF reply signals are available at either set of Sum, Delta, and Omni output channels located at the rear panel of the MBTS. These signals may then be used in a variety of ways to verify radar system performance.

Detailed information concerning Constant Range Ring Mode operation is available in the sections that follow.

2.3.2.1 Constant Range Ring Mode Configuration

To use the Constant Range Ring Mode, the MBTS and the Operator Control Subsystem (OCS) must be configured and activated as indicated in the System Startup description. When the OCS controls the MBTS, the Azimuth Gated Target Mode is the default operating condition. Change to the Constant Range Ring Mode by clicking on the Constant Range Ring Mode control in the Mode Select panel.

The Constant Range Ring Mode OCS control panel appears as shown in Figure 25, the Constant Range Ring Mode OCS Screen. Details concerning the operation of the controls shown in this figure are discussed in the following sections.

The Constant Range Ring Mode Functional Block Diagram, Figure 26, shows how the various OCS controls affect signal characteristics at each MBTS output. Use of these controls is described in the following sections.

2.3.2.2 Constant Range Ring Mode Connections

Pulsed RF signals are available at a variety of MBTS output ports. Output connections are the same as described in the CW Mode. Refer to Section 2.3.1.2.3, 1090 MHz CW Mode Connections for more information.

Trigger signals may be applied to the MBTS in a variety of ways. Complete information regarding connection to and selection of a trigger source can be found in the Trigger Control section of this guide.

Figure 25. Constant Range Ring Mode OCS Screen

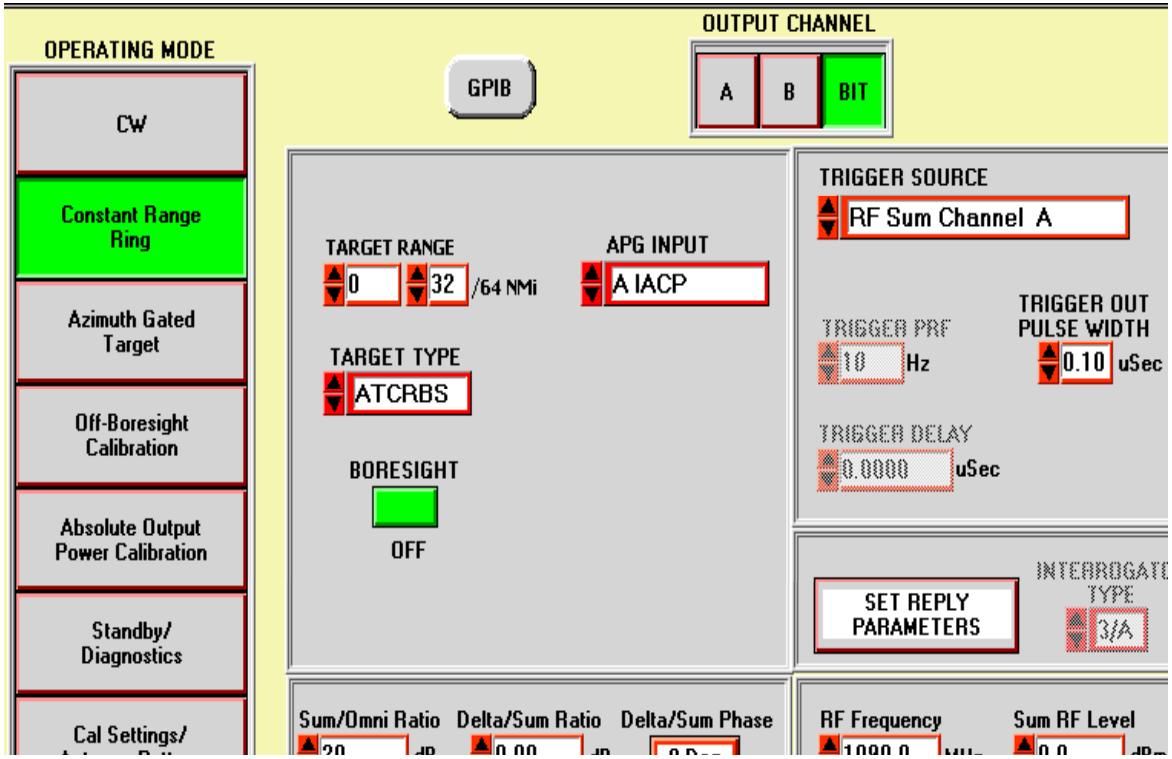
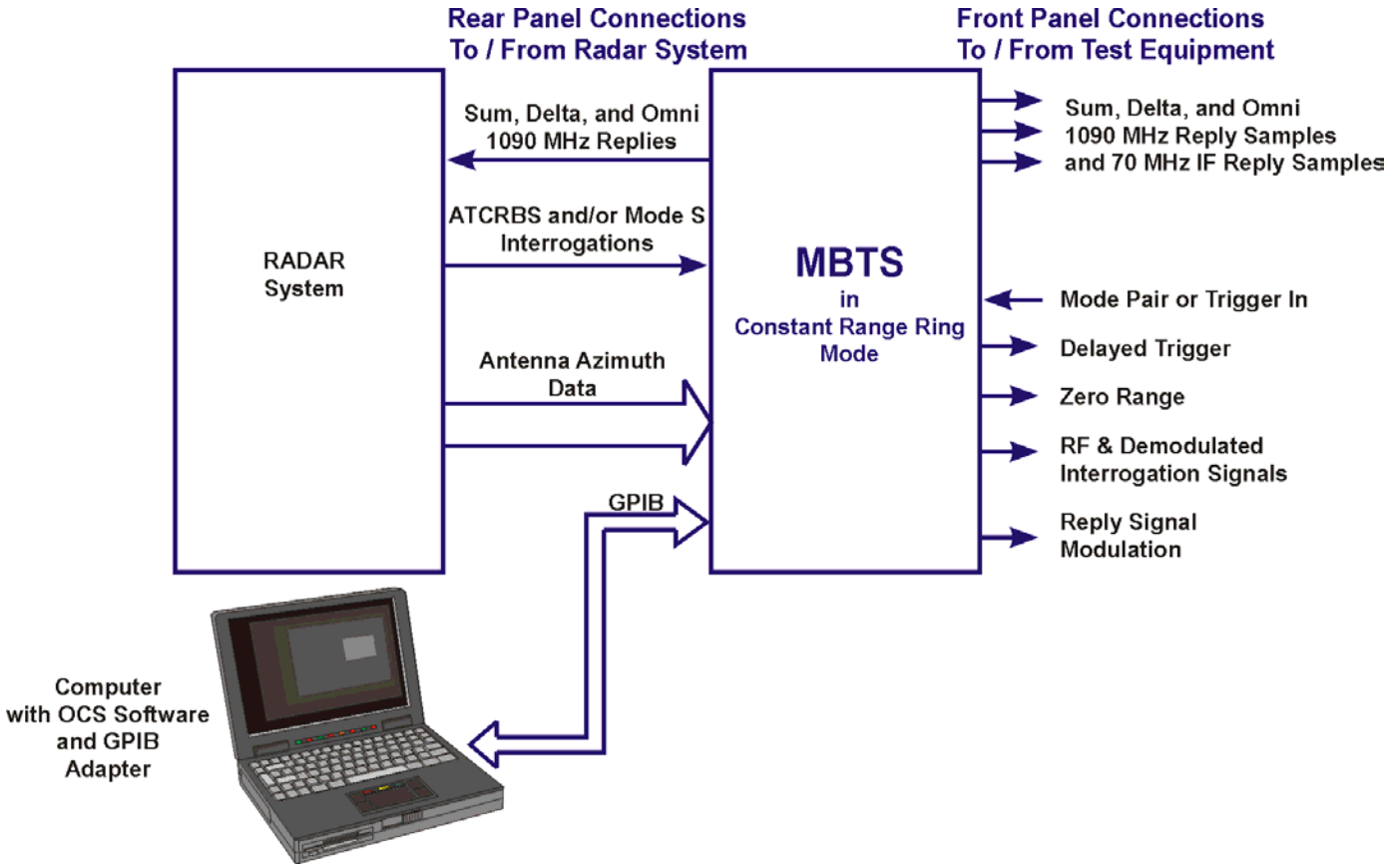


Figure 26. Constant Range Ring Mode Functional Block Diagram



2.3.2.3 Constant Range Ring Mode Controls

The OCS controls shown in Figure 25, the Constant Range Ring Mode OCS Screen, are used to set the operational parameters of pulsed signals generated by the MBTS.

RF Frequency. The OCS RF Frequency control, Figure 16, sets the output frequency of all RF signals. The default operating frequency is 1090.0 MHz. Signal frequency can be adjusted from 1080.0 to 1100.0 MHz, in 0.2 MHz steps.

The IF signal frequency, at the 70 MHz Upconverter Test ports, is always 70 MHz. The frequency of these signals does not vary due to frequency changes made to the RF outputs.

SUM Output Level. The Sum RF Level control, Figure 16, sets the output amplitude of the Channel A and Channel B SUM RF signals. Output signal level can be set to between –85 dBm and +10 dBm, in 0.5 dB increments.

NOTE

The amplitude level of the DELTA and OMNI RF outputs are set relative to the SUM RF Level. Thus, changing the SUM output level also changes the level of the DELTA and OMNI outputs.

DELTA Output Level. The Delta/Sum Ratio control, Figure 17, sets the level of the Delta Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –41.75 to +12.0 dB, in 0.25 dB increments. The Boresight Control can disable the use of the Delta/Sum ratio control.

NOTE

The operator should set the DELTA RF control so as to maintain DELTA RF signals at or between absolute amplitude levels of –110 dBm and +16 dBm. The OCS Delta/Sum control allows settings outside of this range. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

OMNI Output Level. The Sum/Omni ratio control, Figure 17, sets the level of the Omni Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –28 to +20 dB in 1 dB increments.

NOTE

The operator should set the OMNI RF control so as to maintain OMNI RF signals at or between absolute amplitude levels of –105 dBm and -10 dBm. The OCS Sum/Omni control allows settings outside of this range. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

DELTA Output Phase. The Delta/Sum Phase control, Figure 17, sets the phase of the Delta signal channel relative to that of the Sum Channel signal. The control allows selection of either an in-phase state (zero degree) or a 180-degree phase state. Phase matching applies only to the Channel A and B Sum and Delta outputs located on the rear panel of the MBTS. The phase relationship of the 1090 MHz and 70 MHz test output signals is not guaranteed.

Output Channel Selection. Only one output channel, A or B, is active at a time. Output channel selection is made through the use of the Output Select control. RF Output System Status indicators, one on the PCC front panel and the other on the OCS status panel, are GREEN if either output Channel A or output Channel B is selected. If the BIT setting of the Output Select control is selected, both output status indicators will be YELLOW.

NOTE

If there appears to be a signal level problem with the MBTS check the status of the Output Select control. Often no RF output channel has been selected.

Interrogator Type. When the use of external or internal pulse triggers is selected, the Interrogator Type control assigns an interrogator type to the trigger signal. This assignment is required by the MBTS to determine the proper reply response. Interrogator type choices include ATCRBS Type 2, B, C, and 3/A, Mode S All-Call (S), Mode S Roll-Call Altitude (SA), or Mode S Roll-Call ID (SI). The Interrogator Type setting is disregarded when replies are triggered from either RF interrogations or Mode Pair signals.

Set Reply Parameters. Activating the Set Reply Parameters control, Figure 13, opens the Reply Parameter Window. The controls within this window set all user variable code and pulse parameters for each reply type. Refer to the Reply Data Control section for a complete description of this function.

Range. The Range Control sets a delay within the timing circuits of the MBTS such that generated replies properly simulate a target at a range of from 0.5 to 255 nautical miles (nmi). Two control fields set the Range in integer miles, from 0 to 255, and fractional miles, in increments of 1/64 mile.

Range delay calculations are based upon the use of 198 range delay units, of 62.5 nanoseconds each, per mile. This factor simulates the two-way signal

transmission time between the generation of a radar interrogation and the receipt of a transponder reply by the radar system. The time delay specified for the normal processing of ATCRBS and Mode S interrogations by the transponder is in addition to the time delay set by the Range control. This additional timing delay factor, based upon either the actual or assigned interrogation type, is calculated and automatically applied by the MBTS.

The Range control does not affect MBTS amplitude settings.

Target Type. The Target Type control is used to assign a transponder type to the MBTS. Selections include ATCRBS, Mode S, or a 50/50 mix of the two signal types. If either the ATCRBS or the Mode S setting is chosen only ATCRBS or Mode S replies will be generated by the MBTS. If the 50/50 mix selection is made, the MBTS will respond with both ATCRBS and Mode S replies. In this case, if a response from both target types is appropriate, the ATCRBS response will take precedence.

Trigger Source. The Trigger Source control sets MBTS to use the desired trigger signal. Use the Trigger Source link for a detailed description of control settings and operation.

Trigger PRF. The PRF control sets the rate of internally generated triggers from 10 to 1,000 Hertz in 5 Hz increments. The PRF value may be set using either the UP/DOWN controls or by direct keyboard entry. A "TRIG Conflict" message is displayed on the System Status display if the settings of the internal trigger rate control and the range control are incompatible. Trigger status messages are only generated in response to internal Trigger PRF and Range control settings.

Trigger Pulse Width. The Pulse Width control sets the width of the TTL signal at the Trigger Out connector (J16). Control settings are from 0.1 to 5.0 microseconds in 0.1 microsecond increments. The Pulse Width setting is made through the use of either the UP/DOWN controls or by direct keyboard entry.

Trigger Delay. The Trigger Delay control sets a delay between the application of an external trigger pulse and the generation of a trigger signal at the Trigger Out port, J16, of the PCC Module (see Table 17). The trigger delay value can be set from 0.0 to 3.0 milliseconds in increments of 62.5 nanoseconds. The timing of the reply signal is unaffected by this function.

Boresight. When in the ON position the Boresight control sets the Delta/Sum ratio of all MBTS reply signals to a minimum (-36 dB). This condition simulates a target in the middle of the antenna beam pattern. The OFF control setting allows the use of the Delta/Sum ratio control.

APG Input. The APG Input control selects which of the available MBTS rear panel Azimuth Pulse Generator (APG) input signal channels are active. The control also permits manual or automatic selection of input data type, Antenna Change Pulses (ACP) or Improved Azimuth Change Pulses (IACP).

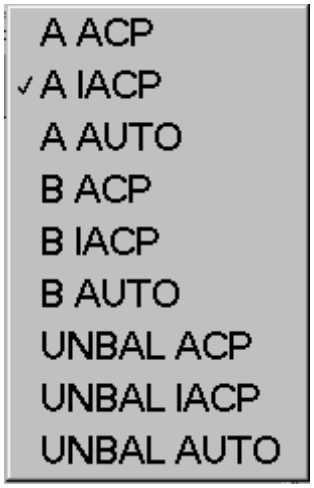
The MBTS includes three sets of APG inputs, which correspond to the selections available on the APG Input control as shown in Figure 27. The APG INPUT A or B (A ACP, A IACP, A AUTO, B ACP, or B IACP, B AUTO) settings select balanced data from the RS-422 Channel A or B input connector J9. The APG UNBAL settings select input data from the 75 Ohm azimuth data input connectors J10 (ACP) and J11 (ARP). If one of the A AUTO, B AUTO, or UNBAL AUTO selections is chosen, the MBTS measures the incoming pulses and automatically determines if the APG source is generating ACP or IACP data pulses.

Azimuth data signals may be applied to connectors J9, J10, and J11 on the Rear Panel of the MBTS. APG input signal specifications are listed in

Sections 4.2.1.3, J9 - RS-422 Balanced APG Data Inputs, and 4.2.1.4, J10 and J11 – 75 Ohm APG Data Inputs, of this manual.

The MBTS does not require APG data inputs to operate in the Constant Range Ring Mode. In this case, however, the Antenna Alarm function must be disabled.

Figure 27. Antenna Pulse Generator (APG) Input Selector



2.3.2.4 Test Signal Ports

Interrogation and reply RF and data signals can be monitored at the numerous front panel test ports of the MBTS. These are described in detail in the sections that follow.

2.3.2.4.1 IDR Module Test Ports

RF Interrogation and demodulated interrogation data signals can be examined at the front panel test connections of the Interrogation Demodulation Receiver (Section 3.2.3) Module.

1030 MHz Interrogation Signal. Signals from the selected RF interrogation input channel may be observed at J21 – 1030 MHz RF Interrogation Test Out port of the IDR Module. Signals at this test port are from 20 to 55 dB below the level of the input signals applied at the rear panel of the MBTS. Refer to the J1 - SUM Channel A Target Reply Output (and SUM Channel A Radar Interrogation Input) and J7 and J8 - Channel A and B Interrogation Inputs sections for more information about interrogation signal characteristics.

Demodulated PAM Signal. The detected pulse amplitude modulation (PAM) characteristics of the interrogation signal may be observed at J22 – PAM Video Test Out port of the IDR Module. This TTL level data signal is the same as that routed to PCC Module for data processing purposes.

Demodulated DPSK Signal. Demodulated DPSK data signals, derived from Mode S interrogations, may be observed at J23 – DPSK Video Test Out port of the IDR Module. This TTL level data signal is the same as that routed to PCC Module for data processing purposes.

LOG Video Signal. The amplitude characteristics of the applied pulsed RF interrogation signals may be observed at J24 – Log Video Test Out port of the IDR Module. The signal level at this output depends upon the amplitude of the applied interrogation signal. The pulsed DC output signal has a logarithmic response to the power level of the applied input signal.

2.3.2.4.2 PCC Module Test Ports and Status Indicators

Reply modulation and reply timing data signals are available at front panel test connections of the PCC Module. Status indicators, also on front panel of the PCC Module, provide important insight into the operating condition of the MBTS. The PCC Module test ports and status indicators are discussed below.

PAM Reply Data. The signal at J17 – PAM Reply Data controls the timing and characteristics of all pulsed RF signals from the MBTS. It is routed directly to the Pulse Amplitude Modulation (PAM) circuit within the Reply Generator Module. A TTL low signal enables the generation of RF output signals from the MBTS.

Phase Reply Data. The signal at J18 – Phase Reply Data controls the phase relationship between the Delta and Sum RF output signals. A TTL high signal sets the Delta and Sum signals to be in an in-phase, 0 degree, state. A TTL low results in a 180 degree relationship.

Zero Range Data. The rising edge of the pulse signal at J19 –Zero Range Data marks the start point, or "zero range", of the range delay time period. This timing mark occurs either 3 μSec, for ATCRBS, or 128 μSec, for Mode S, after the reception of an interrogation signal. The time between a pulse signal at this test port and one at the PAM Reply Data port is determined by the Range control setting. See the discussion on Range for more information. The Zero Range signal does not control any functions internal to the MBTS. It is provided to aid in the test and measurement verification process.

Trigger Out Data. A pulse signal at J16 – Trigger Out is created for every valid trigger signal detected by the MBTS. When the MBTS is triggered from external pulses, a time delay between the triggering pulse and the Trigger Out pulse may be applied. For more information refer to the Trigger Delay function, above.

NOTE

To generate an RF reply the MBTS requires both a valid trigger signal and correlation between the trigger signal type (ATCRBS or Mode S) and the Target Type setting of the MBTS.

Mode/External Trigger. The input J15 – Mode/External Trigger, is the connection through which Mode Pair pulse sequences or pulse triggers are applied to the MBTS. The MBTS will trigger from only Type 2, Type 3/A, Type B, and Type C pulse sequences applied at this port. Mode Pair sequences must comply with the timing characteristics specified in National Air Standard (NAS) documents. Out of tolerance Mode Pair pulses or pulse sequences are ignored by the MBTS.

NOTE

The time between consecutive trigger signals must be greater than time it takes for the MBTS to generate a reply response. Make sure that the MBTS Range setting is appropriate for the repetition rate of the applied trigger signal. The MBTS will ignore trigger signals received while generating a reply from a previously detected trigger.

Mode Indicators. Two rows of Mode Indicators on the front panel of the PCC Module display the trigger and reply status of the MBTS.

The row of indicators on the left displays the type of valid trigger signal detected by the MBTS. A valid trigger causes the LED associated with the trigger to momentarily turn GREEN. Two or more indicators may be illuminated if interleaved interrogation sequences are applied to the MBTS.

The indicators on the right display the type of reply signals generated by the MBTS. The Target Type control sets the type of reply signal the MBTS will generate for a given trigger signal. The association between trigger signal type and reply response type follows transponder requirements as stated in National Air Standard guidelines. For external or internal pulse triggers the Reply Data Control assigns a trigger type to the trigger signal.

2.3.3 Azimuth Gated Target Mode

When in the Azimuth Gated Target Mode the MBTS generates pulsed RF replies in response to trigger signals that occur when the azimuth position of the radar antenna correlates with the location of a target simulated by the MBTS. The amplitude of the Sum, Delta, and Omni pulsed reply signals vary, based upon antenna pattern characteristics and upon the timing of the received trigger signal. A constellation of from one to thirty-two simulated targets can be created by the MBTS. Unlike the Ring Mode of operation, reply generation is gated by target position.

While in this mode the MBTS generates replies in response to ATCRBS or Mode S RF interrogations, ATCRBS mode pair triggers, and external triggers. The trigger signal input is selected through the use of the Trigger Source control. The Target Type control sets the MBTS to simulate an ATCRBS target, a Mode S target, or a 50/50 mix of both ATCRBS and Mode S targets. The Range control sets the timing of the MBTS reply to properly simulate a target at a range of from 0.5 to 255 nautical miles (nmi). A number of other controls set target location parameters, antenna pattern characteristics, and Azimuth Pulse Generator (APG) input channel.

The pulsed RF reply signals are available at either set of Sum, Delta, and Omni output channels located at the rear panel of the MBTS. These signals may then be used in a variety of ways to verify radar system performance.

Detailed information concerning Azimuth Gated Target Mode operation is available in the sections that follow.

2.3.3.1 Azimuth Gated Target Mode Configuration

To use the Azimuth Gated Target Mode, the MBTS and the Operator Control Subsystem (OCS) must be configured and activated as indicated in the System Startup description. When the OCS controls the MBTS, the Azimuth Gated Target Mode is the default operating condition.

The Azimuth Gated Mode OCS control panel appears as shown in Figure 28, the Azimuth Gated Target Mode OCS Screen. Details concerning the operation of the controls shown in this figure are discussed in the following sections.

Figure 29, the Azimuth Gated Target Mode Function Block Diagram shows how the various OCS controls affect signal characteristics at each MBTS output. Use of these controls is described in the following sections.

2.3.3.2 Azimuth Gated Target Mode Connections

Pulsed RF reply signals are available at a variety of MBTS output ports. Output connections are the same as described in the CW Mode. Refer to Section 2.3.1.2.3, 1090 MHz CW Mode Connections for more information.

Trigger signals may be applied to the MBTS in a variety of ways. Complete information regarding connection to and selection of a trigger source can be found in the Trigger Control section of this manual.

Balanced or unbalanced APG signals must be applied to the rear panel APG input connections of the MBTS. The APG Input section provides more details on how to configure and select these inputs.

Figure 28. Azimuth Gated Target Mode OCS Screen

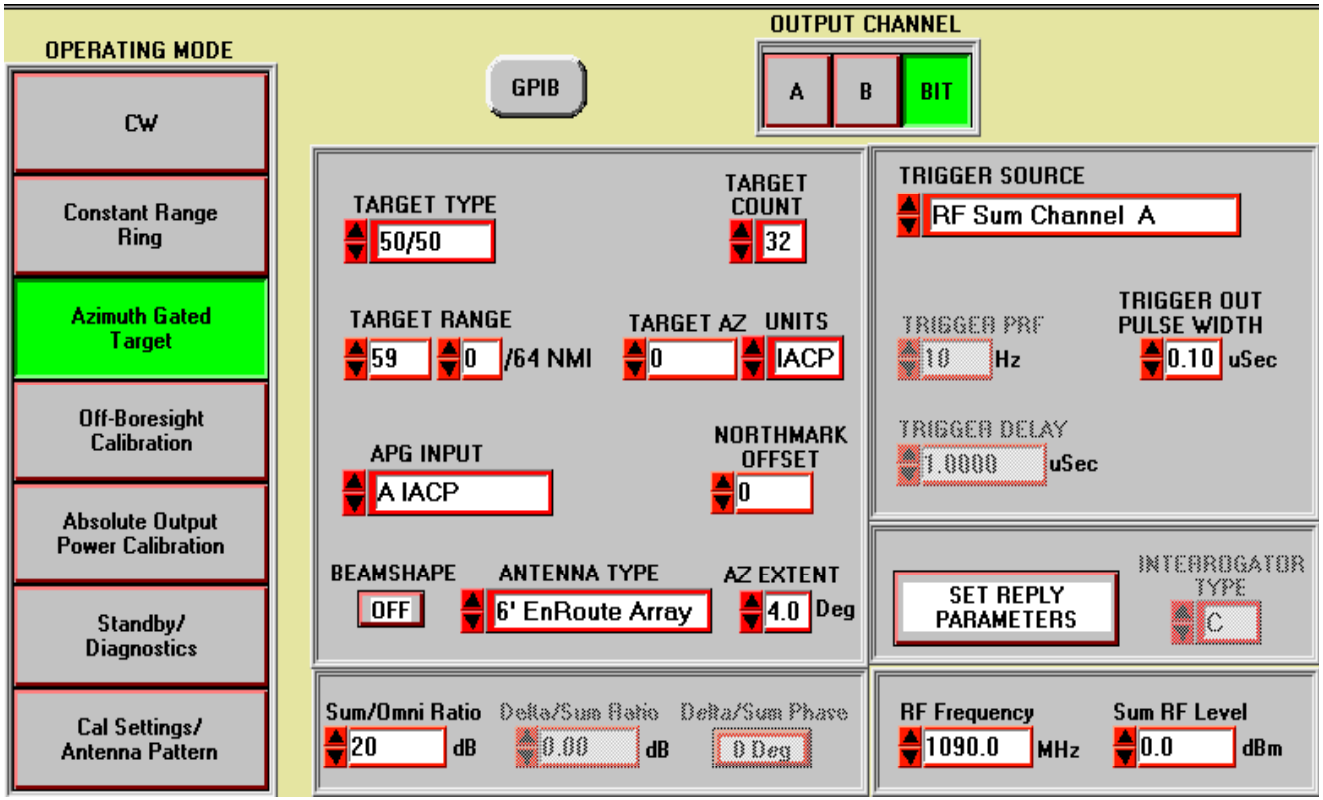
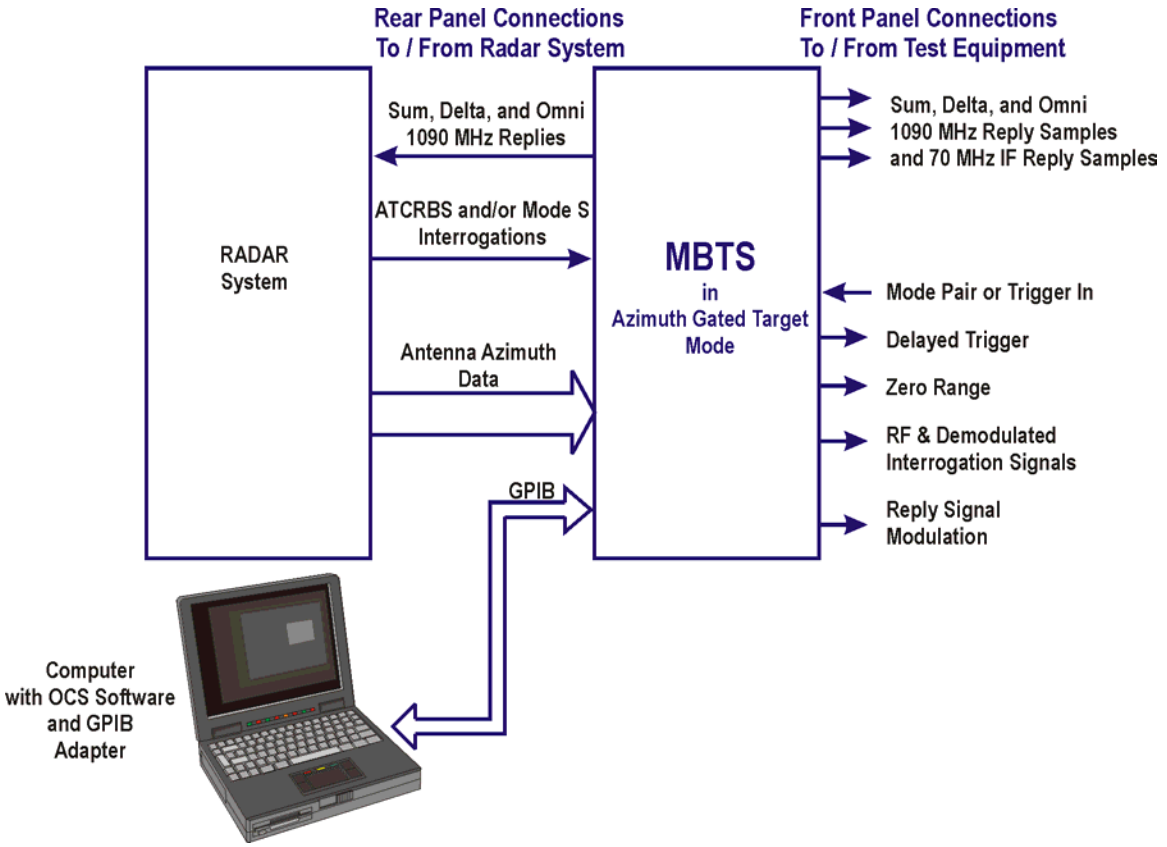


Figure 29. Azimuth Gated Target Mode Function Block Diagram



2.3.3.3 Azimuth Gated Target Mode Controls

The OCS controls shown in Figure 28, the Azimuth Gated Target Mode OCS Screen, are used to set the operational parameters of pulsed signals generated by the MBTS.

RF Frequency. The OCS RF Frequency control, Figure 16, sets the output frequency of all RF signals. The default operating frequency is 1090.0 MHz. Signal frequency can be adjusted from 1080.0 to 1100.0 MHz, in 0.2 MHz steps.

The IF signal frequency, at the 70 MHz Upconverter Test ports, is always 70 MHz. The frequency of these signals does not vary due to frequency changes made to the RF outputs.

SUM Output Level. The Sum RF Level control, see Figure 16, sets the output amplitude of the Channel A and Channel B SUM RF signals. The output signal level can be set to between –85 dBm and +10 dBm in 0.5 dB increments.

NOTE

The amplitude level of the DELTA and OMNI RF outputs are set relative to the SUM RF Level. Thus, changing the SUM output level also changes the level of the DELTA and OMNI outputs.

NOTE

Slightly higher levels of wideband RF noise are present at MBTS outputs when the SUM RF Level setting is at or above –54 dBm. When operating within 6 dB of this signal level be aware that the properties of the selected antenna pattern may cause reply signals from the MBTS to vary in noise content. Setting the Azimuth Extent control to less than or equal to 3.6 degrees, and the Beamshape control to OFF, eliminates this condition.

DELTA Output Level. The Delta/Sum Ratio control, Figure 17, sets the level of the Delta Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –41.75 to +12.0 dB in 0.25 dB increments. For the Azimuth Gated Mode, this control is only active when the MANUAL antenna type selection is made. When operating in the Azimuth Gated Mode, the MBTS normally calculates the required Delta/Sum ratio automatically.

NOTE

The operator should set the DELTA RF control so as to maintain DELTA RF signals at or between absolute amplitude levels of –110 dBm and +16 dBm. The OCS Delta/Sum control allows settings outside of this range. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

OMNI Output Level. The Omni Output Level control, see Figure 17, sets the level of the Omni Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –28 to +20 dB in 1 dB increments.

NOTE

The operator should set the OMNI RF control so as to maintain OMNI RF signals at or between absolute amplitude levels of –105 dBm and -10 dBm. The OCS Sum/Omni control allows settings outside of this range. When amplitude settings exceed the capability of the MBTS an "Amplitude Conflict" message is displayed in the System Status window (see Figure 7).

DELTA Output Phase. The Delta/Sum Phase control, see Figure 17, sets the phase of the Delta signal channel relative to that of the Sum Channel signal. The control allows selection of either an in-phase state (zero degree) or a 180-degree phase state. Phase matching applies only to the Channel A and B Sum and Delta outputs located on the rear panel of the MBTS. The phase relationship of the 1090 MHz and 70 MHz test output signals is not guaranteed. For the Azimuth Gated Mode, this control is only active when the MANUAL antenna type selection is made. The MBTS normally sets the required Delta/Sum phase state automatically when operating in the Azimuth Gated Mode.

Output Channel Selection. Only one output channel, A or B, is active at a time. Output channel selection is made through the use of the Output Select control. RF Output System Status indicators, one on the PCC front panel and the other on the OCS status panel, are GREEN if either output Channel A or output Channel B is selected. If the BIT setting of the Output Select control is selected, both output status indicators will be YELLOW.

NOTE

If there appears to be a signal level problem with the MBTS check the status of the Output Select control. Often no RF output channel has been selected.

Interrogator Type. When the use of external pulse triggers is selected, the Interrogator Type control assigns an interrogator type to the trigger signal. This assignment is required by the MBTS to determine the proper reply response. Interrogator type choices include ATCRBS Type 2, B, C, and 3/A, Mode S All-Call (S), Mode S Roll-Call Altitude (SA), or Mode S Roll-Call ID (SI). The Interrogator Type setting is disregarded when replies are triggered from either RF interrogations or Mode Pair signals.

Set Reply Parameters. Activating the Set Reply Parameters control, as seen in Figure 13, opens the Reply Parameter Window. The controls within this window set all user variable code and pulse parameters for each reply type. Refer to the Reply Data Control section for a complete description of this function.

Range. The Range Control sets a delay within the timing circuits of the MBTS such that generated replies properly simulate a target at a range of from 0.5 to 255 nautical miles (nmi). Two control fields set the Range in integer miles, from 0 to 255, and fractional miles, in increments of 1/64 mile.

Range delay calculations are based upon the use of 198 range delay units, of 62.5 nanoseconds each, per mile. This factor simulates the two-way signal transmission time between the generation of a radar interrogation and the receipt of a transponder reply by the radar system. The time delay specified for the normal processing of ATCRBS and Mode S interrogations by the transponder is in addition to the time delay set by the Range control. This additional timing delay factor, based upon either the actual or assigned interrogation type, is calculated and automatically applied by the MBTS.

The Range control does not affect MBTS amplitude settings.

Target Type. The Target Type control is used to assign a transponder type to the MBTS. Selections include ATCRBS, Mode S, or a 50/50 mix of the two signal types. If either the ATCRBS or the Mode S setting is chosen only ATCRBS or Mode S replies will be generated by the MBTS. If the 50/50 mix selection is made, the MBTS will respond with both ATCRBS and Mode S replies. In this case, if a response from both target types is appropriate, the ATCRBS response will take precedence.

Trigger Source. The Trigger Source control sets MBTS to use the selected trigger signal. For the Azimuth Gated Mode, the internal trigger selection is disabled.

Trigger Pulse Width. The Pulse Width control sets the width of the TTL signal at the Trigger Out connector (J16). Control settings are from 0.1 to 5.0 microseconds in 0.1 microsecond increments. The Pulse Width setting is made through the use of either the UP/DOWN controls or by direct keyboard entry.

Trigger Delay. The Trigger Delay control sets a delay between the application of an external trigger pulse and the generation of a trigger signal at the Trigger Out port, J16, of the PCC Module (see Table 17). The trigger delay value can be set from 0.0 to 3.0 milliseconds in increments of 62.5 nanoseconds. The timing of the reply signal is unaffected by this function.

APG Input. The APG Input control selects which of the available MBTS rear panel Azimuth Pulse Generator (APG) input signal channels are active. The control also permits manual or automatic selection of input data type, Antenna Change Pulses (ACP) or Improved Azimuth Change Pulses (IACP). ***Valid APG data is mandatory for the MBTS to operate in the Azimuth Gated Target Mode.***

The MBTS includes three sets of APG inputs, which correspond to the selections available on the APG Input control as shown in Figure 27. The APG Channel A or B input settings (A ACP, A IACP, A AUTO, B ACP, or B IACP, B AUTO) select balanced data from the RS-422 Channel A or B input connector J9. The APG UNBAL settings select input data from the 75 Ohm azimuth data input connectors J10 (ACP) and J11 (ARP). If one of the A AUTO, B AUTO, or UNBAL AUTO selections is chosen, the MBTS measures the incoming pulses and automatically determines if the APG source is generating ACP or IACP data pulses.

Azimuth data signals are applied to connectors J9, J10, and J11 on the Rear Panel of the MBTS. APG input signal specifications are listed in Sections 4.2.1.3, J9 – RS-422 Antenna Azimuth Data Inputs, and 4.2.1.4, J10 and J11 – 75 Ohm APG Data Inputs, of this manual.

The Antenna Alarm function may be enabled or disabled.

First Target Azimuth. The First Target Azimuth control sets the azimuth location of the "first", or reference, target. The azimuth location of any additional targets is determined relative to the position of the first target. The First Target Azimuth setting can be in degrees (0 to 359), in ACP units (0 to 4095), or in IACP units (0 to 13683). The Target Azimuth Units control determines which of the three unit choices is applied.

All targets are placed so as to create an evenly spaced target constellation. For example, if the Target Count control is set to four, the target separation is 90 degrees. If the first target is located at an azimuth of 45 degrees, the second target is centered at 135 degrees, the third target is centered at 225 degrees, and the fourth target is centered at 315 degrees.

Target Azimuth Units. The Target Azimuth Units control selects the azimuth radial units applied to the first target location. Available settings include DEG (degrees), ACP, or IACP. The azimuth location of the first target is automatically recalculated and loaded into the MBTS if a change in the azimuth unit setting is altered.

Northmark Offset. The Northmark Offset control is used to rotate the position of each target in the MBTS target constellation so that replies from the MBTS are aligned with the orientation of the radar system. The Northmark Offset control setting is in IACP units only. Entering an offset rotates the position of the first target, and of the entire target constellation, relative to the azimuth location marked by the ARP signal. The Northmark Offset value can be from 0 to 16383 in IACP units.

Target Count. The number of simulated targets can be set to 1, 2, 4, 8, 16, or 32. The targets are evenly distributed over the full 360 degrees of an antenna rotation. For example, if four targets are chosen, they are spaced every 90 degrees. Sixteen targets are spaced every 22.5 degrees.

Antenna Type. The Antenna Type control is used to select which of the antenna beam patterns stored in memory is used by the MBTS to formulate reply signals. Five different control choices are available. These include the ASR-11/MSSR LVA, the Five Foot Terminal Array, the Six Foot EnRoute Array, a User Defined pattern, and a MANUAL setting. The antenna pattern characteristics of the first three choices, the ASR-11/MSSR LVA, the Five Foot Terminal Array, and the Six Foot EnRoute Array are based upon the measured performance of each array type. These patterns are permanently stored in MBTS memory.

The User Defined pattern, as delivered from FSE, does not simulate performance that can be achieved by an antenna. This pattern can be, and should be, calibrated to match the characteristics of the antenna at the site where the MBTS is installed (see the Off-Boresight Calibration Mode for more information on this topic). After calibration, the User Defined pattern stored in the MBTS will closely match the monopulse characteristics of the radar system. The use of this selection will then result in the most accurate and stable calculation of target location (by the radar system).

NOTE

After calibration to the radar system, the User Defined selection will always set the MBTS to generate reply signals with the most accurate and stable monopulse characteristics.

The Manual control selection permits the operator to set the MBTS to generate replies with a fixed Delta/Sum amplitude ratio at a fixed Delta/Sum phase relationship. When this selection is made the Delta/Sum Ratio and the Delta/Sum Phase controls within the Delta and Omni Output Signal Controls window are activated.

Azimuth Extent. The Azimuth Extent control sets the beamwidth of the selected antenna pattern. Target replies from the MBTS are not generated unless the difference between the position of the antenna pedestal and the position of an MBTS target is less than or equal to one half of the Azimuth Extent setting. Azimuth Extent can be set from 2.0 to 5.0 degrees in 0.2 degree increments.

Beamshape. The Beamshape control sets the Sum Channel amplitude response across the extent of the selected antenna pattern. The MBTS will create replies that have a flat Sum Channel response, from beam edge to beam edge, when the Beamshape control is OFF. In this case the amplitude of all Sum Channel reply signals will be as set by the Sum RF Level control. The MBTS creates Sum Channel signal replies that follow the amplitude characteristics of the selected Antenna Type pattern when the Beamshape control is ON. In this case reply signal amplitude matches the Sum RF Level setting only when the azimuth position of the system antenna is aligned with the azimuth location of an MBTS target.

The Beamshape control setting does not affect the monopulse characteristics (Delta/Sum ratio or phase) of the reply signals generated by the MBTS.

2.3.3.4 Test Signal Ports

Interrogation and reply RF and data signals can be monitored at the numerous front panel test ports of the MBTS. These are described in detail in the sections that follow.

2.3.3.4.1 IDR Module Test Ports

RF Interrogation and demodulated interrogation data signals can be examined at the front panel test connections of the Interrogation Demodulation Receiver (IDR) Module. Refer to Section 2.3.2.4.1, IDR Module Test Ports, for a full description of these test ports.

2.3.3.4.2 PCC Module Test Ports and Status Indicators

Reply modulation and reply timing data signals are available at front panel test connections of the PCC Module. Status indicators, also on front panel of the PCC Module, provide important insight into the operating condition of the MBTS. The PCC Module test ports and status indicators are discussed below. Refer to Section 2.3.2.4.2, PCC Module Test Ports and Status Indicators, for a full description of these test ports.

2.3.4 Off-Boresight Calibration Mode

When in the Off-Boresight Calibration Mode the MBTS generates pulsed RF replies in response to all valid Type 3/A ATCRBS trigger signals. The amplitude of the Sum and Omni pulsed reply signals is fixed at operator selectable settings. The amplitude response of the Delta Channel signal is automatically determined by the MBTS. The amplitude setting of the Delta Channel signal is encoded into the ATCRBS reply data generated by the MBTS. The Delta Channel output level, and the corresponding encoded response data pattern, is updated for each response generated such that all valid monopulse settings are transmitted. The reply pattern sequence, as well as reply data encoding, is described below. The "X" bit in the reply data sequence is enabled to mark the presence of this special reply signal. Reply generation is not gated by target position as it is in the Azimuth Gated Target Mode.

The encoded replies from the MBTS can be used to create a site-specific antenna pattern for the MBTS. The use of this antenna pattern enables the MBTS to generate reply signals that yield a very low target jitter when plotted by the radar system. The process that calibrates the MBTS to the radar system is as follows. When in the Off-Boresight Calibration Mode the MBTS generates pulsed RF replies in which the monopulse setting of a reply sequence is encoded into the reply data transmission. The reply data from the MBTS is recorded and analyzed by the radar system. A new User Defined antenna pattern (see the Antenna Type section) is created and loaded into the MBTS that calibrates the output characteristics of the MBTS to the antenna and receiver characteristics of the radar system. This enables the MBTS to generate target responses that the radar system can use to formulate accurate and repeatable target fixes.

While in this mode of operation the MBTS generates replies only in response to ATCRBS Type 3/A RF interrogations or ATCRBS Type 3/A mode pair triggers. The MBTS will not reply to either internal or external triggers. The trigger signal input is selected through the use of the Trigger Source control. The Target Type control is fixed at the ATCRBS setting. Any valid Range control setting may be used.

The pulsed RF reply signals are available at either set of Sum, Delta, and Omni output channels located at the rear panel of the MBTS.

Detailed information concerning Off-Boresight Calibration Mode operation is available in the sections that follow.

2.3.4.1 Off-Boresight Calibration Mode Configuration

To use the Off-Boresight Calibration Mode, the MBTS and the Operator Control Subsystem (OCS) must be configured and activated as indicated in the System Startup description. When the OCS controls the MBTS, the Azimuth Gated Target Mode is the default operating condition. Change to the Off-Boresight Calibration Mode by clicking on the Off-Boresight Calibration Mode control in the Mode Select Panel.

The Off-Boresight Calibration Mode OCS control panel appears as shown in Figure 30 the Off-Boresight Calibration Mode OCS Screen. Details concerning the operation of the controls shown in this figure are discussed in the following sections.

Figure 30. Off-Boresight Calibration Mode Screen

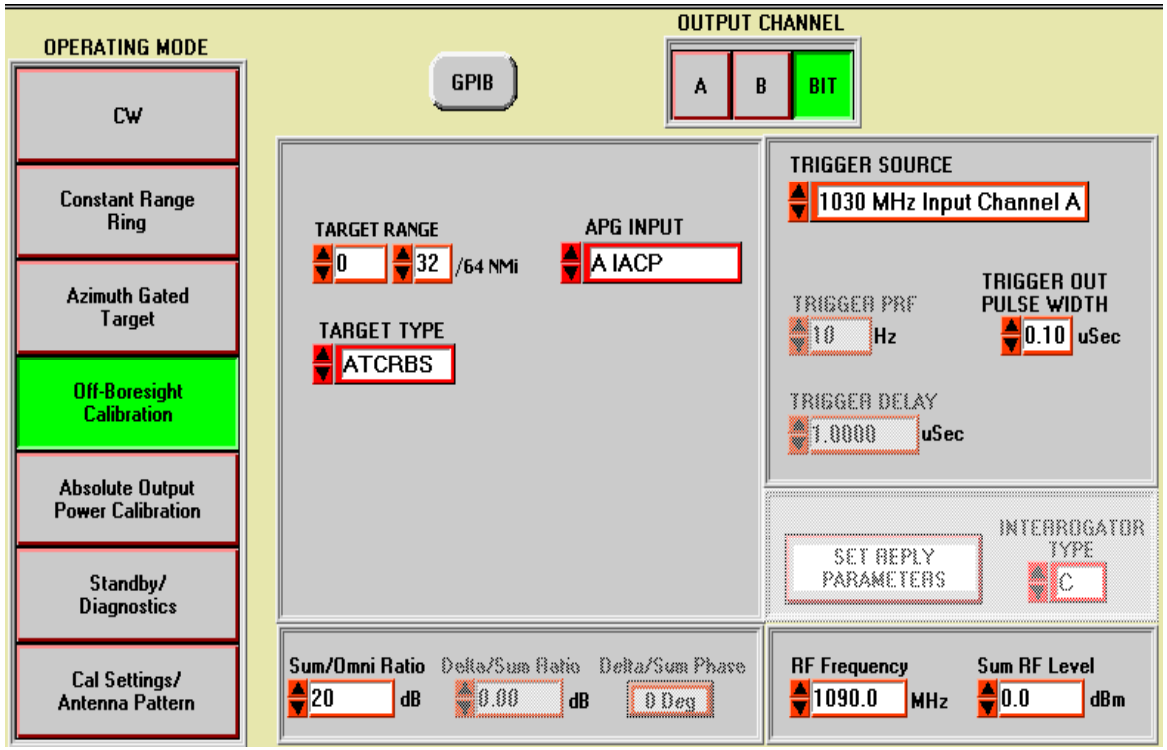


Figure 31. Off-Boresight Calibration Mode Block Diagram

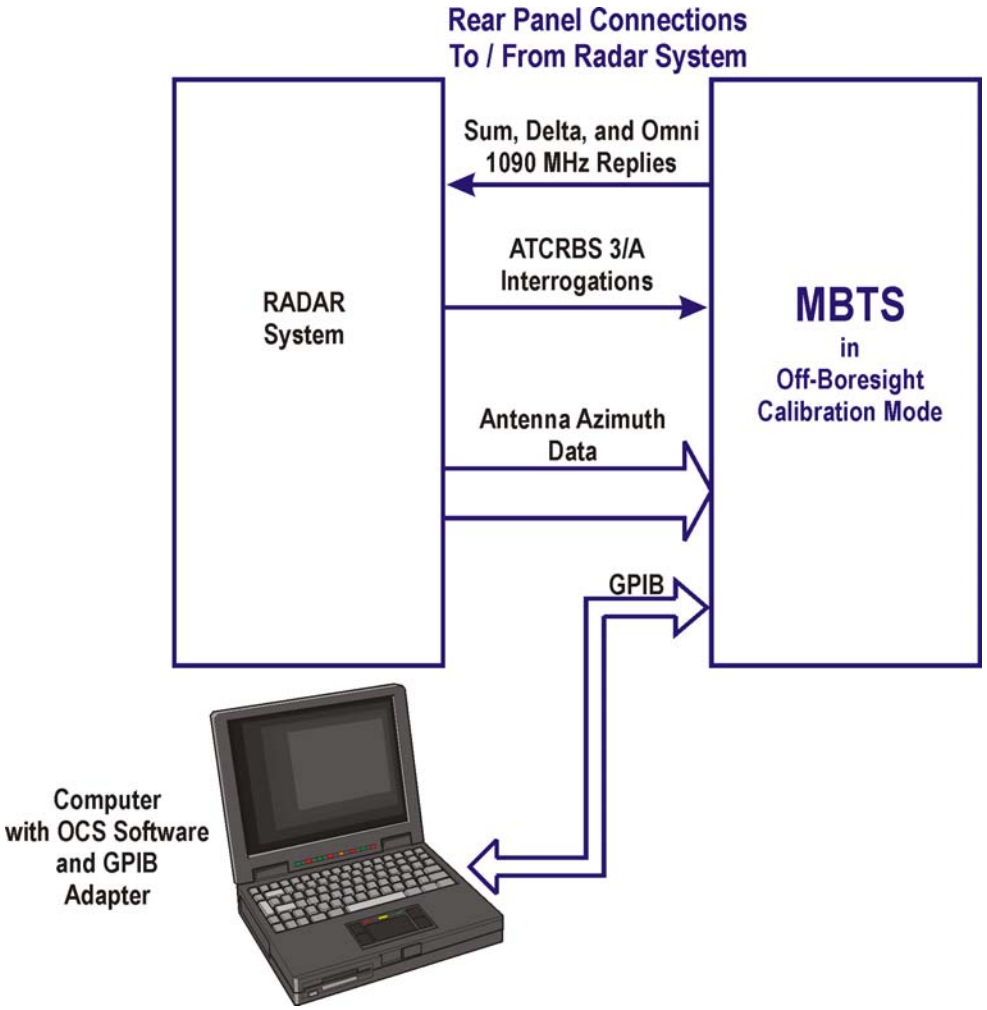


Figure 31, the Off-Boresight Calibration Mode Function Block Diagram shows how the various OCS controls affect signal characteristics at each MBTS output. Use of these controls is described in the following sections.

2.3.4.2 Off-Boresight Calibration Mode Connections

Pulsed RF signals are available at a variety of MBTS output ports. Output connections are the same as described in the CW Mode. Refer to Section 2.3.1.2.3, 1090 MHz CW Mode Connections for more information.

Trigger signals may be applied to the MBTS in a variety of ways. Complete information regarding connection to and selection of a trigger source can be found in the Trigger Control section of this manual. In this mode the MBTS cannot be set to reply to either internal or external triggers.

The MBTS does not require APG data inputs to operate in the Off-Boresight Calibration Mode. In this case, however, the Antenna Alarm function must be disabled. The APG Input section describes the available data input connections and the use of the APG control.

2.3.4.3 Off-Boresight Calibration Mode Controls

The OCS controls shown in Figure 30, the Off-Boresight Calibration Mode OCS Screen, are used to set the operational parameters of pulsed signals generated by the MBTS.

RF Frequency. The OCS RF Frequency control, Figure 16, sets the output frequency of all RF signals. The default operating frequency is 1090.0 MHz. Signal frequency can be adjusted from 1080.0 to 1100.0 MHz, in 0.2 MHz steps.

The IF signal frequency, at the 70 MHz Upconverter Test ports, is always 70 MHz. The frequency of these signals does not vary due to frequency changes made to the RF outputs.

SUM Output Level. The Sum RF Level control, see Figure 16, sets the output amplitude of the Channel A and Channel B SUM RF signals. The output signal level can be set to between –85 dBm and +10 dBm in 0.5 dB increments. For the Off-Boresight Calibration Mode the Sum RF Level control should be set at or above –20 dBm to allow proper characterization of the Delta Channel signal.

NOTE

The amplitude level of the DELTA and OMNI RF outputs are set relative to the SUM RF Level. Thus, changing the SUM output level also changes the level of the DELTA and OMNI outputs.

OMNI Output Level. The Sum/Omni Ratio control, see Figure 17, sets the level of the Omni Channel signal relative to that of the Sum Channel signal. The adjustment range of this control is from –28 to +20 dB in 1 dB increments.

NOTE

The operator should set the OMNI RF control so as to maintain OMNI RF signals at or between absolute amplitude levels of –105 dBm and -10 dBm. The OCS Sum/Omni control allows settings outside of this range.

Output Channel Selection. Only one output channel, A or B, is active at a time. Output channel selection is made through the use of the Output Select control. RF Output System Status indicators, one on the PCC front panel and the other on the OCS status panel, are GREEN if either output Channel A or output Channel B is selected. If the BIT setting of the Output Select control is selected, both output status indicators will be YELLOW.

NOTE

If there appears to be a signal level problem with the MBTS check the status of the Output Select control. Often no RF output channel has been selected.

Range. The Range Control sets a delay within the timing circuits of the MBTS such that generated replies properly simulate a target at a range of from 0.5 to 255 nautical miles (nmi). Two control fields set the Range in integer miles, from 0 to 255, and fractional miles, in increments of 1/64 mile.

Range delay calculations are based upon the use of 198 range delay units, of 62.5 nanoseconds each, per mile. This factor simulates the two-way signal transmission time between the generation of a radar interrogation and the receipt of a transponder reply by the radar system. The time delay specified for the normal processing of ATCRBS and Mode S interrogations by the transponder is in addition to the time delay set by the Range control. This additional timing delay factor, based upon either the actual or assigned interrogation type, is calculated and automatically applied by the MBTS.

The Range control does not affect MBTS amplitude settings.

Trigger Source. The Trigger Source control sets the MBTS to use the selected trigger signal. For the Off-Boresight Calibration Mode, the internal and external trigger selections are disabled.

2.3.4.4 Off Boresight Calibration Mode Data Encoding

The MBTS can achieve Delta-to-Sum output signal ratios from +12 dB to –41.75 dB, in 0.25 dB steps. The Delta/Sum phase relationship may be set to either 0º or to 180º. This performance is achieved in the MBTS through the use and implementation of a number of GaAs attenuator integrated circuits. A total of 432 reply sequences from the MBTS are required to cover all valid combinations of Delta/Sum amplitude and phase control settings.

Eleven amplitude control bits and one phase control bit are utilized by the monopulse controls within the MBTS. These are identified in Table 1 below. The attenuator section is active (higher signal loss) when the reply includes the indicated encoded pulse. The phase control is set to 180º when the encoded pulse is present. To calculate the MBTS D/S ratio setting from an encoded reply, total the Function value assigned to each received pulse, as indicated below, and add the sum to 6.0 dB. For instance, if a reply sequence included the B1, C2, and D4 pulses the D/S setting of the MBTS is 6.0 + (-16.0 + -4.0 + -1.0) dB = -15 dB. Note that no encoded pulses (except possibly the phase pulse) are transmitted when the D/S ratio is 6.0 dB.

While in the Off-Boresight Mode the MBTS will continuously cycle through the entire set of valid monopulse settings.

NOTE

To insure accurate results, the MBTS should be allowed to warm up for at least 30 minutes prior to the start of any calibration process.

Table 1. Monopulse Data Encoding

Control Label	Function	Encode Pulse ID	Comment
D/S 0.25 dB	-0.25 dB Atten	D1	
D/S 0.5 dB	-0.5 dB Atten	D2	
D/S 1.0 dB	-1.0 dB Atten	D4	
D/S 2.0 dB	-2.0 dB Atten	C1	
D/S 4.0 dB	-4.0 dB Atten	C2	
D/S 8.0 dB	-8.0 dB Atten	C4	
D/S 16.0 dBA	-16.0 dB Atten	B1	
D/S 16.0 dBB	-16.0 dB Atten	B2	
Aux D/S 1.0 dB	+1.0 dB Atten	B4	Used for D/S > 6.0 dB
Aux D/S 2.0 dB	+2.0 dB Atten	A1	Used for D/S > 6.0 dB
Aux D/S 4.0 dB	+4.0 dB Atten	A2	Used for D/S > 6.0 dB
Phase	Phase	A4	180º when pulse is present

2.3.5 Absolute Output Power Calibration Mode

The Absolute Output Power Calibration Mode is used to automatically create a new output level calibration file. This file, when loaded into the MBTS, aligns the achieved output signal level of the MBTS with the indicated output level setting over the full dynamic range of signal level control.

At each MBTS output level setting, the OCS adjusts attenuator circuits within the MBTS, and through the use of a measurement feedback loop, determines the best attenuator control value for the signal level setting. Because the output level control circuits of the MBTS have a resolution 0.25 dB, an overall accuracy of much less than the required 0.5 dB is usually achieved.

In addition to the MBTS and the OCS, the calibration process requires the use of an HP-8902A Measuring Receiver (with an HP 11722A Power Sensor). The OCS controls the entire measurement process, including the HP-8902 and the MBTS, through an IEEE-488 interface.

2.3.5.1 Absolute Output Power Calibration Mode Configuration

During the calibration process, measurement and control signals are communicated between the OCS, the MBTS, and the HP-8902 over an IEEE-488 interface. The required bus addresses for these are: for the OCS, the system controller, address 0; for the MBTS, address 1; and for the HP-8902, address 14.

The HP-8902 Tuned Receiver section must be calibrated prior to beginning the Off-Boresight Calibration process. Refer to the HP-8902 User's Manual for information on this topic.

To use the Absolute Output Power Calibration Mode, the MBTS and the Operator Control Subsystem (OCS) must be configured and activated as indicated in the System Startup description. When the OCS controls the MBTS, the Azimuth Gated Target Mode is the default operating condition. Change to the Absolute Output Power Calibration Mode by clicking on the Absolute Output Power Calibration Mode control in the Mode Select Panel.

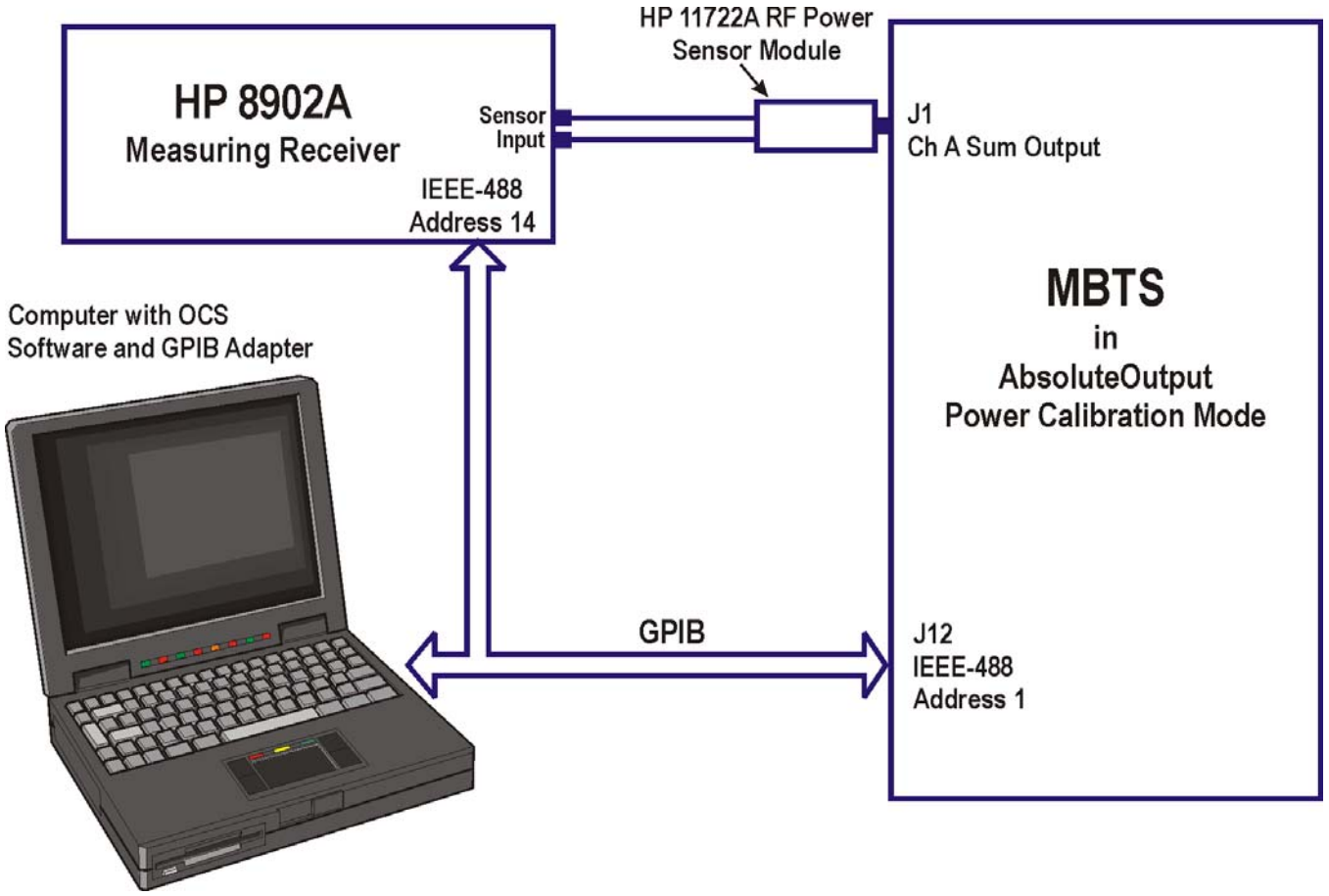
NOTE

Most calibration factors cannot be changed unless the Configuration Switch on the side of the PCC Module is set to allow this operation. This condition is indicated by a red "Write Protected" display in the top-center of the Cal settings/Antenna Patterns Mode window. The two files that are used to formulate a User Defined antenna pattern, Beamshape and Boresight, can be uploaded into the MBTS independent of the Configuration Switch setting. Refer to Section 3.2.6.2.1 for information on configuring the MBTS to accept calibration files.

2.3.5.2 Absolute Output Power Calibration Mode Connections

Figure 32, the Absolute Output Power Calibration Setup indicates how the OCS, the MBTS, and the HP-8902 should be configured. Make sure that Bus addresses are as indicated and that bus interconnect cables are attached to each interface port. The 11722A Power Sensor must be connected to the Channel A Sum Output connector, J1 (refer to the MBTS Rear Panel illustration for connector locations).

Figure 32. Absolute Output Power Calibration Test Setup



2.3.5.3 Absolute Output Power Calibration Mode Controls and Operation

The Absolute Output Power Calibration Mode OCS control panel appears as shown in Figure 33. Clicking on the Calibrate control starts the measurement process.

For each MBTS output power level setting between +10.0 dBm and –85.0 dBm a best-fit attenuation setting is determined. These attenuator settings are recorded on the OCS hard drive. As the process advances the Sum Level indicator changes from +10 dBm to –85 dBm, and the progress bar fills in. The measurement process requires about 30 minutes. It is complete when the –85 dBm level is reached.

Two calibration files are created in the C:\OCS folder, Raw Levels.txt and Power Info.txt. The Raw Levels file is in the proper format for uploading into the MBTS using the process explained in Section 2.3.7.3, UPLOAD CAL TARGET TABLE. The Power Info.txt file is formatted so that the calibration results can be easily reviewed and analyzed. ***The Power Info.txt should be reviewed before the Raw Levels file is uploaded into the MBTS.*** The HP-8902 can generate erroneous readings if its tuned receiver is out of alignment.

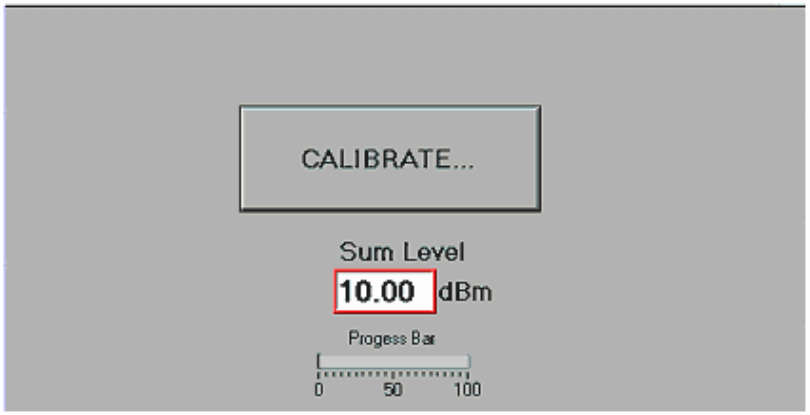
Once the Raw Levels.txt file is loaded into the MBTS, the output level accuracy of the MBTS will be within ±0.5 dB of the power level setting. This can be verified by running the *Target Level Measurement Exe* program located in the C:\OCS folder. This program uses the HP-8902 to measure the output level of the MBTS at each output level setting. The equipment setup is exactly as described above. However, before the target level measurement program is run, the MBTS should be placed in CW Mode and the OCS program exited.

Test results are placed in the Target level Measurements.txt file in the C:\Test folder. This file is formatted so that the measurement results can be easily reviewed and analyzed. ***Always verify calibration results before using the MBTS instrument.***

NOTE

To insure accurate results, the MBTS and Measuring Receiver must warm up for a minimum of 30 minutes prior to performing this calibration.

Figure 33. Absolute Output Power Calibration Screen



2.3.6 Standby/Diagnostics Mode

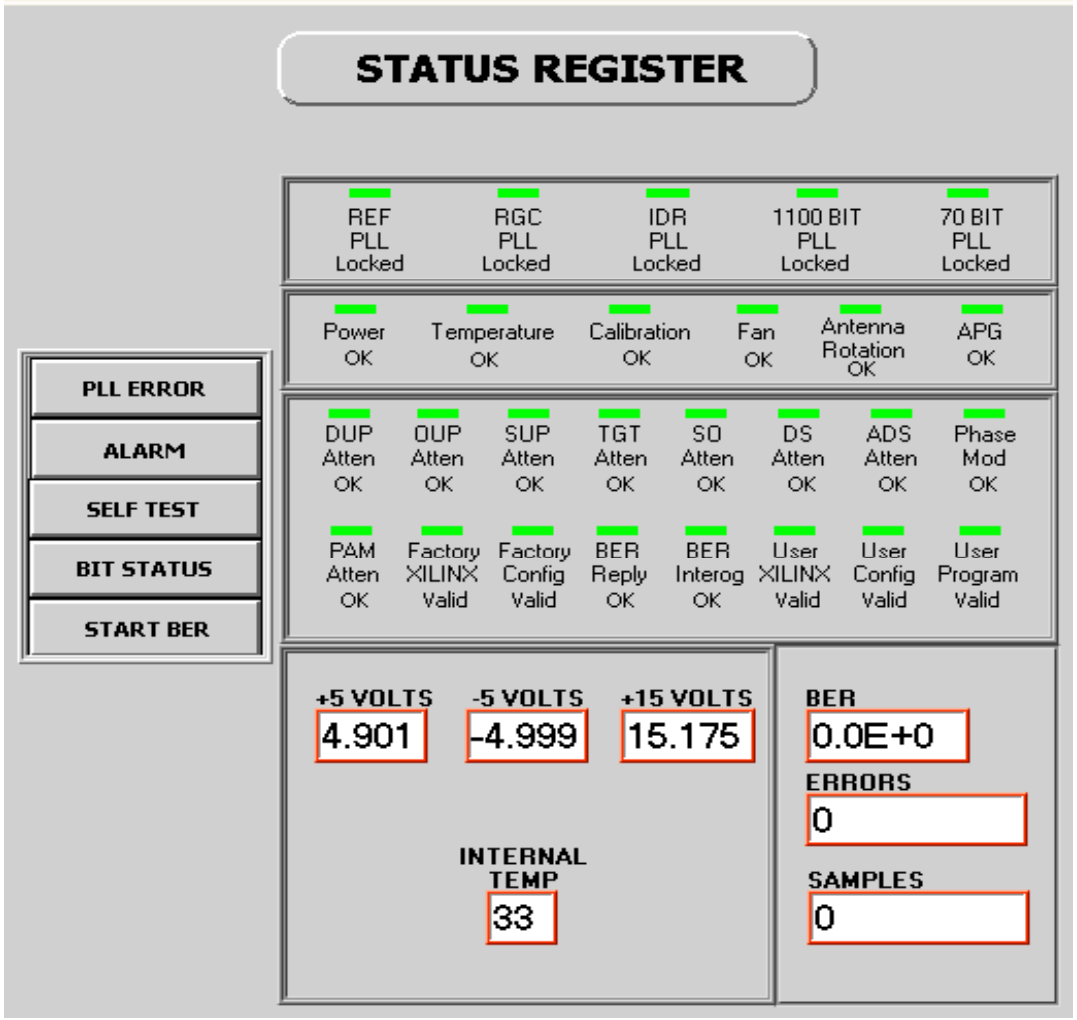
When the Standby/Diagnostics Mode is selected, the OCS first places the MBTS into a standby operating state and then automatically runs a series of self-check diagnostic routines. The details of the test results are displayed as shown in Figure 34. The results can be used to analyze and investigate operational problems of the MBTS (see Section 5.2 for more information). If a problem is indicated in the System Status panel the operator should use this mode to begin problem diagnosis.

This operational mode displays the results of all Built-In-Test (BIT) functions. All output amplitude or phase setting controls are monitored by BIT. Other functions that are monitored include power supply voltages, phase lock status of all PLL circuits, internal temperature, APG status, processor status, and memory functions. Controls are available to start a BER loop test and to initiate a new self-test routine. Additional information on diagnosing MBTS operational issues is found in the Trouble Diagnostics section of this manual.

2.3.6.1 Standby/Diagnostics Mode Configuration

To use the Standby/Diagnostics Mode, the MBTS and the Operator Control Subsystem (OCS) must be configured and activated as indicated in the System Startup description. When the OCS controls the MBTS, the Azimuth Gated Target Mode is the default operating condition. To change to the Standby/Diagnostics Mode click on the Standby/Diagnostics Mode control in the Mode Select Panel.

Figure 34. Standby/Diagnostics Display



2.3.6.2 Standby/Diagnostics Mode Configuration

The Standby/Diagnostics Mode has no special setup or configuration requirements.

A red "LOADING CURRENT VALUES" message displays for approximately 15 seconds when this mode is first activated. During this period the BIT function checks the performance of all control circuits. The results of the BIT process are displayed when all tests are complete.

2.3.6.3 Standby/Diagnostics Mode Controls and Operation

The Standby/Diagnostics Mode OCS control panel appears as shown in Figure 34. The use of these controls is explained in the following sections.

PLL ERROR. Clicking the PLL ERROR control updates the status of the five PLL indicators in the Phase Locked Loop (PLL) Status Panel of the indicator panel display.

ALARM. Clicking on the ALARM control updates the status of the six Equipment Status Indicators on the indicator panel display.

SELF TEST. Clicking on SELF TEST control starts a new BIT sequence. All major MBTS system functions are evaluated. When complete, test results are displayed in the BIT Function Status Panel. Test failures are indicated by a RED status display.

BIT STATUS. Clicking the BIT STATUS button updates the status of the power supply voltage readouts and the chassis internal temperature display in the Power Supply and Chassis Temperature panel.

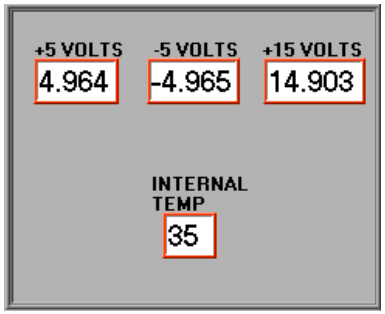
START BER. Clicking the START BER control begins a Bit Error Rate (BER) test process. The BER loop includes the generation of interrogation signals by the BIT Module, the demodulation of these signals by the IDR Module, and an evaluation of the demodulated data by the PCC Module. The PCC Module controls the entire BER test process. It records the number of errors detected and the total number of data samples. These, along with a calculated BER, are displayed in the lower right hand corner of Figure 34.

The BER test process continues indefinitely until the STOP BER control is used (the START BER control changes to STOP BER after the BER process begins). ***Any displayed error indicates an equipment problem.*** Additional information on diagnosing MBTS operational issues is found in the Trouble Diagnostics section of this manual.

2.3.6.4 Standby/Diagnostics Mode Status Indicators

The definition of each of the status indicators displayed on the Standby/Diagnostics Display panel, Figure 34, is given below. In all cases, a green indicator means that the circuit is functioning normally. Abnormal circuit function is indicated by a red display. Trouble analysis recommendations, based upon the status of the display indicators, are found in the Trouble Diagnostics section of this manual.

2.3.6.4.1 Power Supply and Chassis Temperature Panel



The lower center of the display screen includes readouts for the three power supply voltages and for the chassis internal temperature. Clicking on the BIT STATUS control refreshes the voltage and temperature readings.

Voltage Indicators. The measured output voltage of each power supply is indicated. The outputs of the ±5V supply are expected to be within ±0.25 volts of the rated value. The output of the +15V supply is expected to be within ±0.5 of the rated value. If any of the supply voltages fall out of the expected operational window then a BIT PWR ALARM is generated (see the Equipment Status Indicators section). Power supply voltage measurements can be verified at the MBTS Front Panel test points.

Do not operate the MBTS if power supply voltages are out of tolerance.

Temperature Indicator. The measured internal temperature of the MBTS is indicated. The MBTS will operate with an internal temperature between 0°C and +65°C. If the measured temperature falls out of the design window then a BIT TEMP ALARM is generated (see the Equipment Status Indicators section). Note: After warm-up the internal temperature of the MBTS is 10 Cº to 15 Cº above ambient.

Do not operate the MBTS if the ambient or internal temperatures exceed design tolerances.

2.3.6.4.2 Phase Locked Loop (PLL) Status Panel

The upper-most display panel reports the Phase Lock status for each of the PLL circuits in the MBTS. A green status display indicates a normal operating state. A red status display indicates an unlocked condition.

Do not operate the MBTS if PLL circuit failures are indicated. Trouble analysis recommendations, based upon the status of the display indicators, are found in the Trouble Diagnostics section of this manual.

REF PLL. The status of the PLL circuit within the Reference Source Module is indicated. The REF PLL circuit generates the LO signal for each of the three Upconverter Modules. The output frequency of the MBTS will be in doubt if the REF PLL indicator is red.

RGC PLL. The status of the PLL circuit within the Reply Generator Module is indicated. The RGC PLL circuit generates the primary output signal of the MBTS. The output frequency of the MBTS will be in doubt if the RGC PLL indicator is red.

IDR PLL. The status of the PLL circuit within the Interrogation Demodulator Module is indicated. The IDR PLL circuit generates the LO signal that translates the 1030 MHz interrogation signals down to an IF at 60 MHz. The ability of the MBTS to properly decode interrogations will be in doubt if the IDR PLL indicator is red.

1100BIT PLL. The status of the 1100 MHz PLL circuit within the BIT Module is indicated. The 1100BIT PLL circuit generates the LO signal that converts the 70 MHz BIT interrogation signals to 1030 MHz. The ability of the BIT Module to generate interrogations will be in doubt if the 1100BIT PLL indicator is red.

70BIT PLL. The status of the 70 MHz PLL circuit within the BIT Module is indicated. The 70BIT PLL circuit generates the primary interrogation signal of the BIT Module. The ability of the BIT Module to generate interrogations will be in doubt if the 70BIT PLL indicator is red.

2.3.6.4.3 Equipment Status Indicators

The middle display panel reports the status of some general operating conditions of the MBTS. A green status display indicates a normal operating state. A red status display indicates an unlocked condition.

BIT Pwr Alarm. The status of the power supplies within the MBTS is indicated (see Section 2.3.6.4.1). If any of the three power supply voltages is out of tolerance a fault condition will be displayed.

Do not operate the MBTS if power supply voltages are out of tolerance.

BIT Temp Alarm. The status of the internal temperature of the MBTS is indicated (see Section 2.3.6.4.1). If the internal temperature is not within 0ºC and 65ºC a fault condition will be displayed.

Do not operate the MBTS if the ambient or internal temperatures exceed design tolerances.

Cal Failed. The status of the Sum Channel temperature compensation process is indicated. A failure means that the output level of the MBTS may not meet specification requirements. Operation of the MBTS is possible, but not recommended when output level accuracy is important.

Fan Failed. The status of the cooling fan inside the MBTS is indicated. A failure means that the fan has stopped rotating. Operation of the MBTS is possible, but not recommended since fan failure may lead to heat stress of circuits internal to the MBTS.

ANT ROT Alarm. The equivalent rotation rate of the applied APG signals is indicated. The MBTS expects the antenna platform to spin at a rate of between 4 and 15 revolutions per minute. A failure means that these tolerances have been exceeded.

An ANT ROT Alarm will also generate an OCS front panel ANT ALARM (see Section 2.2.10). The ANT ROT Alarm will not hinder MBTS operation if the ANT ALARM function is disabled.

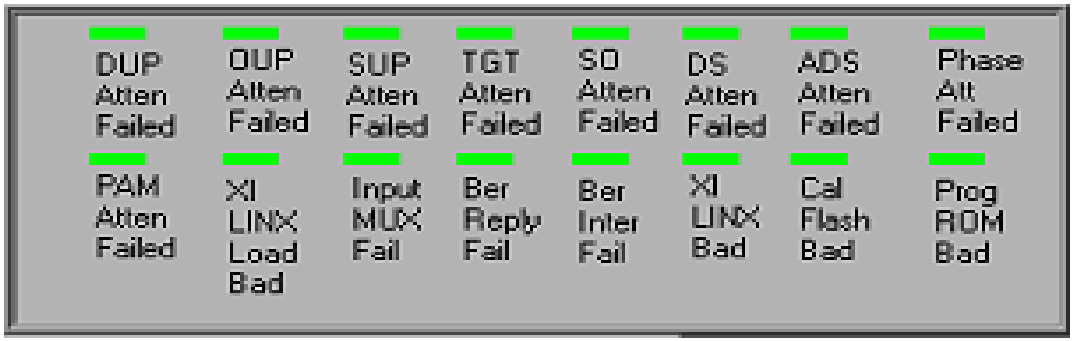
APG Alarm. The condition of antenna ARP and ACP data signals is indicated. The MBTS expects the ratio (and timing) of ACP pulses to ARP pulses to fall within fairly tight tolerances (4096 ±2 or 16384 ±2). A failure means that these tolerances have been exceeded.

An APG Alarm will also generate an OCS front panel ANT ALARM (see Section 2.2.10). The APG Alarm will not hinder MBTS operation if the ANT ALARM function is disabled. However, improper APG data will lead to inconsistent target reply generation in the Azimuth Gated Target Mode.

2.3.6.4.4 BIT Function Status Panel

The BIT Function Status Panel indicates the detailed results of the BIT process. A green status display indicates a normal operating state. A red status display indicates an unlocked condition.

Operation of the MBTS with any BIT Function Status failure is not recommended. Trouble analysis recommendations, based upon the status of the display indicators, are found in the Trouble Diagnostics section of this manual.



DUP Atten Failed. The condition of the attenuator circuits within the Delta Channel Upconverter Module is indicated. The characteristics of five attenuator circuits (0.5dB, 1 dB, 2 dB, 4 dB, and 8 dB) are verified. A failure means that one or more of the attenuator circuits are problematic.

OUP Atten Failed. The condition of the attenuator circuits within the Omni Channel Upconverter Module is indicated. The characteristics of five attenuator circuits (0.5dB, 1 dB, 2 dB, 4 dB, and 8 dB) are verified. A failure means that one or more of the attenuator circuits are problematic.

SUP Atten Failed. The condition of the attenuator circuits within the Sum Channel Upconverter Module is indicated. The characteristics of five attenuator circuits (0.5dB, 1 dB, 2 dB, 4 dB, and 8 dB) are verified. A failure means that one or more of the attenuator circuits are problematic.

TGT Atten Failed. The condition of the target level attenuator circuits within the Reply Generator Module and the Sum Channel Upconverter Module is indicated. The characteristics of nine attenuator circuits (0.25 dB, 0.5dB, 1 dB, 2 dB, 4 dB, 8 dB, 16 dB, 32 dB, and 32 dB) are verified. The final 32 dB step exists within the Sum Channel Upconverter. A failure means that one or more of the attenuator circuits are problematic.

SO Atten Failed. The condition of the Sum/Omni ratio setting attenuator circuits within the Reply Generator Module is indicated. The characteristics of six attenuator circuits (1 dB, 2 dB, 4 dB, 8 dB, 16 dB, and 32 dB) are verified. A failure means that one or more of the attenuator circuits are problematic.

DS Atten Failed. The condition of the Delta/Sum ratio setting attenuator circuits within the Reply Generator Module is indicated. The characteristics of seven attenuator circuits (0.25 dB, 0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, 16 dB, and 16 dB) are verified. A failure means that one or more of the attenuator circuits are problematic.

ADS Atten Failed. The condition of the Aux Delta/Sum ratio setting attenuator circuits within the Reply Generator Module is indicated. The characteristics of six attenuator circuits (2 each of 1 dB, 2 dB, and 4 dB) are verified. A failure means that one or more of the attenuator circuits are problematic.

Phase Modulator Failed. The condition of the phase modulator circuit within the Reply Generator Module is indicated. The ability of the circuit to perform a 0º to 180º phase shift is verified. A failure means that the phase modulator circuit is problematic.

PAM Atten Failed. The condition of the pulse amplitude modulator circuit within the Reply Generator Module is indicated. The ability of the circuit to generate amplitude modulated signals is verified. A failure means that the PAM circuit is problematic.

XILINX Load Bad. The ability of the PCC Module to download a program pattern into the Xilinx FPGA is indicated. A failure means that either the Xilinx FPGA data in the FLASH ROM is corrupt or that there is a problem with the Xilinx hardware.

Flash CAL Bad. The status of stored factory calibration constants is indicated. A failure means that the FLASH ROM sector that stores calibration constants is corrupt.

BER Reply Fail. Not used in present configuration.

BER Inter Fail. The status of interrogation BER measurement process is indicated. Signals are generated in the BIT Module, demodulated by the IDR Module, and analyzed in the PCC Module. A failure means that a BER of less than $1x10^{-4}$ was measured.

XILINX Bad. The status of the user programmable sector of the Xilinx FPGA (within the PCC Module) is indicated. A failure means that there is a problem with the Xilinx FPGA hardware.

Cal Flash Bad. The status of the calibration constant sector of the FLASH ROM (within the PCC Module) is indicated. A failure means that this program area did not pass its checksum test.

Prog ROM Bad. The status of the user program sector of the FLASH ROM (within the PCC Module) is indicated. A failure means that this program area did not pass its checksum test.

2.3.7 Cal Settings/Antenna Patterns Mode

When selected, the Cal Settings/Antenna Patterns Mode displays a window that includes tools for uploading new calibration data and User Defined antenna pattern files into the MBTS. The Cal Settings / Antenna Patterns Data window, as shown in Figure 35, also displays all of the calibration factors currently in use by the MBTS. The use of the controls and an explanation of the displayed information are given below.

WARNING

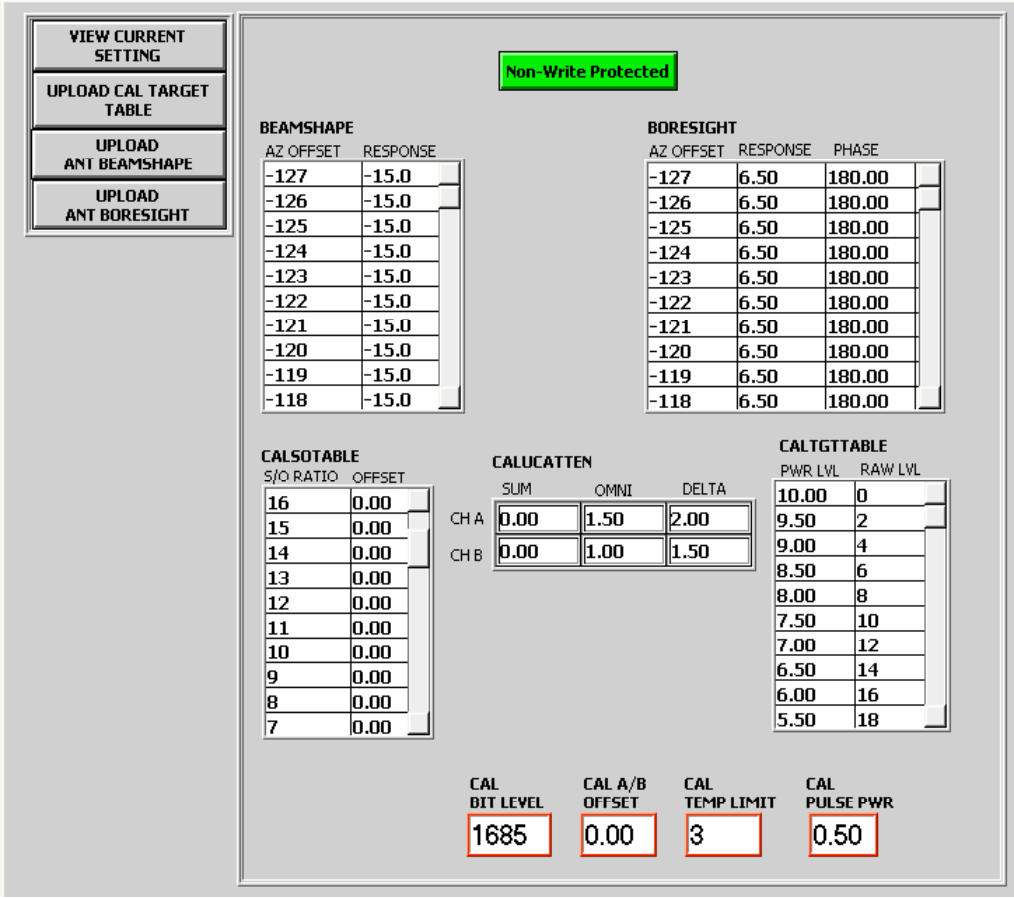
Changing the calibration and antenna parameters of the MBTS can significantly alter the performance of the MBTS. Do not make any such changes without a thorough understanding of the processes involved.

2.3.7.1 Cal Settings/Antenna Patterns Mode Configuration

To use the Cal Settings/Antenna Patterns Mode, the MBTS and the Operator Control Subsystem (OCS) must be configured and activated as indicated in the System Startup description. When the OCS controls the MBTS, the Azimuth Gated Target Mode is the default operating condition. To change to the Cal Settings/Antenna Patterns Mode click on the Cal settings/Antenna Patterns Mode control in the Mode Select Panel.

To change the calibration factors or antenna characteristics of the MBTS the files that contain the new information must be properly formatted. File format requirements are explained in the Monopulse Beacon Test Set IEEE-488 Command Set, FSE document number 100606.

Figure 35. Cal Settings / Antenna Patterns Data Display



NOTE

Most calibration factors cannot be changed unless the Configuration Switch on the side of the PCC Module is set to allow this operation. This condition is indicated by a red "Write Protected" display in the top-center of the Cal settings/Antenna Patterns Mode window. The two files that are used to formulate a User Defined antenna pattern, Beamshape and Boresight, can be uploaded into the MBTS independent of the Configuration Switch setting. Refer to Section 3.2.6.2.1 for information on configuring the MBTS to accept calibration files.

2.3.7.2 Cal Settings/Antenna Patterns Mode Connections

The Cal Settings/Antenna Patterns Mode has no special setup or configuration requirements. Calibration information may be transferred from the OCS to the MBTS through the IEEE-488 interface, J12, through the use of GPIB commands. The data transfer may also take place through the rear panel serial I/O connector, J13 (refer to the MBTS Rear Panel illustration for connector locations). Most users find that file transfers are easier to accomplish using the serial port. Serial interface commands are identical in format to the GPIB commands.

2.3.7.3 Cal Settings/Antenna Patterns Mode Controls and Operation

The Cal Settings/Antenna Patterns Mode OCS control panel appears as shown in Figure 35. The use of these controls is explained in the following sections.

VIEW CURRENT SETTING. The VIEW CURRENT SETTING control refreshes all of the displayed information. The information displayed in the Cal Settings/Antenna Patterns screen is not automatically updated after changes are made to any of the calibration settings. Clicking the VIEW CURRENT SETTING control retrieves and displays the latest data stored in the non-volatile memory of the MBTS.

UPLOAD CAL TARGET TABLE. This control allows a new output level calibration table, called a CALTGTTABLE in the GPIB command set, to be chosen and uploaded into the MBTS. The calibration file created in the Absolute Output Power Calibration Mode, Raw Levels.txt, is properly formatted for this process.

Clicking on the UPLOAD CAL TARGET TABLE control starts the upload sequence. Any properly formatted file may be selected and uploaded, not just the Raw Levels.txt file. File format requirements are listed in the CALTGTTABLE command description within the IEEE-488 Command Set document. After an appropriate file is selected, the file transfer is completed in less than one second. Use the VIEW CURRENT SETTING control to update the displayed CALTGTTABLE information. Verify that the new MBTS settings reflect the information in the file used in the upload process.

UPLOAD ANT BEAMSHAPE. This control allows one of the two files which make a User Defined antenna pattern to be selected and uploaded into the MBTS. The Beamshape file defines the response characteristics of the Sum Channel antenna pattern. It includes amplitude information for 256 adjacent IACP azimuth locations. The file must be formatted as described in the BEAMSHAPE command description of the IEEE-488 Command Set document.

Clicking on the UPLOAD ANT BEAMSHAPE control starts the upload sequence. Any properly formatted file may be selected and uploaded. After an appropriate file is selected, the file transfer is completed in less than one second. Use the VIEW CURRENT SETTING control to update the displayed BEAMSHAPE information. Verify that the new MBTS settings reflect the information in the file used in the upload process.

A new Beamshape file is typically created after running the MBTS in the Off-Boresight Calibration Mode.

UPLOAD ANT BORESIGHT. This control allows one of the two files which make a User Defined antenna pattern to be selected and uploaded into the MBTS. The Boresight file defines the response characteristics, amplitude and phase, of the Delta Channel antenna pattern. It includes amplitude and phase information for 256 adjacent IACP azimuth locations. The file must be formatted as described in the BORESIGHT command description of the IEEE-488 Command Set document.

Clicking on the UPLOAD ANT BORESIGHT control starts the upload sequence. Any properly formatted file may be selected and uploaded. After an appropriate file is selected, the file transfer is completed in less than one second. Use the VIEW CURRENT SETTING control to update the displayed BORESIGHT information. Verify that the new MBTS settings reflect the information in the file used in the upload process.

A new Boresight file is typically created after running the MBTS in the Off-Boresight Calibration Mode.

CALSOTABLE DISPLAY. This display indicates the current setting of this calibration parameter. The values within the CALSOTABLE file are applied as a correction factor to the circuits that set the Sum output level of the MBTS for

each S/O ratio setting. The correction factors keep the absolute level of the Sum Channel output signal within specified requirements.

It is ***not recommended*** that the settings within this calibration table be altered from factory set values. However, a new CALSOTABLE file may be created and loaded into the MBTS. Use the information contained in Sections 2.3.7.1, Cal Settings/Antenna Patterns Mode Configuration, and 2.3.7.2, Cal Settings/Antenna Patterns Mode Connections, as a guideline.

CALUCATTEN DISPLAY. This display indicates the current setting of this calibration parameter. The values within the CALUCATTEN file are applied to correct normal manufacturing variations in the signal gain through each of the three Upconverter signal paths (Sum, Delta, and Omni), and output channels (A and B). The correction factors are applied to the attenuator circuits with each Upconverter. The applied values keep the amplitude of all three output signals within specified requirements.

It is ***not recommended*** that the settings within this calibration table be altered from factory set values. However, a new CALUCATTEN may be created and loaded into the MBTS. Use the information contained is Sections 2.3.7.1 and 2.3.7.2 as a guideline.

CAL BIT LEVEL DISPLAY. This display indicates the current setting of this calibration parameter. The CAL BIT LEVEL setting is used to correct the output level of the MBTS whenever temperature changes are detected.

It is ***not recommended*** that this calibration setting be altered from factory set values. However, a new CAL BIT LEVEL may be created and loaded into the MBTS. Use the information contained is Sections 2.3.7.1 and 2.3.7.2 as a guideline.

CAL A/B OFFSET DISPLAY. This display indicates the current setting of this calibration parameter. The CAL A/B OFFSET setting is used to align the Channel A and B output levels.

It is ***not recommended*** that this calibration setting be altered from factory set values. However, a new CAL A/B OFFSET may be created and loaded into the MBTS. Use the information contained is Sections 2.3.7.1 and 2.3.7.2 as a guideline.

CAL TEMP LIMIT DISPLAY. This display indicates the current setting of this calibration parameter. The CAL TEMP LIMIT value sets the range, in ºC, through which the operating temperature of the MBTS may vary without causing a yellow CALIBRATION alarm (see Section 2.2.1.4). The center of this range is the temperature of the MBTS when the last temperature calibration was performed.

It is ***not recommended*** that this calibration setting be altered from factory set values. However, a new CAL TEMP LIMIT may be created and loaded into the MBTS. Use the information contained is Sections 2.3.7.1 and 2.3.7.2 as a guideline.

3 TECHNICAL DESCRIPTION

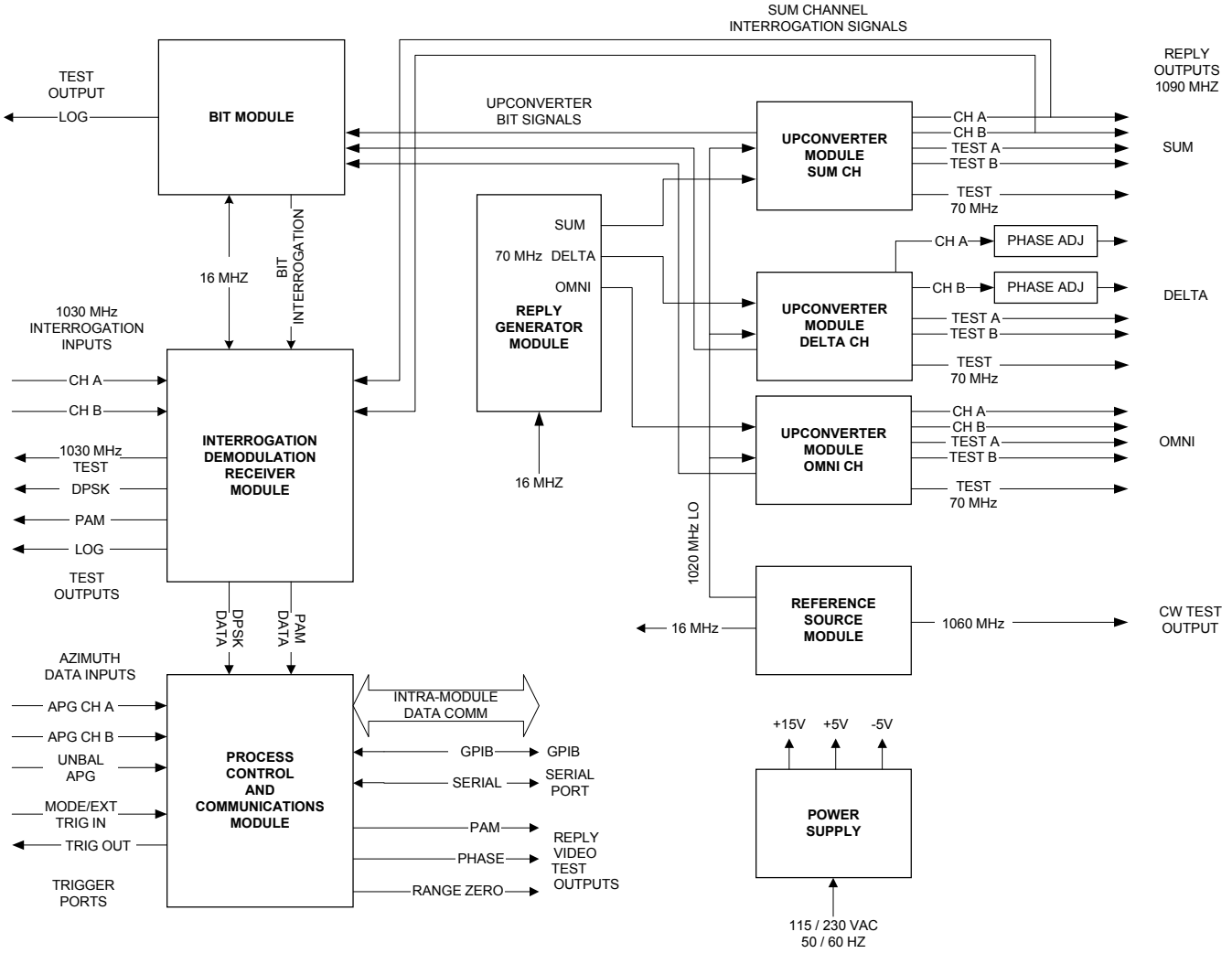
3.1 MBTS Theory of Operation

The MBTS System Block Diagram, Figure 36, illustrates the RF signal paths and other signal interconnections within the MBTS. As indicated by the Block Diagram, the MBTS contains eight modules; one Reply Generator Module, three Upconverter Modules, one Reference Source Module, one Interrogation Demodulation Receiver (IDR) Module, one Built In Test (BIT) Module, and one Process Control and Communications (PCC) Module. The function of each module is briefly described in the following text.

The PCC Module controls all functions within the MBTS. It contains circuits that process received interrogation and azimuth data from which reply responses are created in real time. It processes all user GPIB or serial commands. And, it monitors the status of all RF processes. Refer to the Process Control and Communications (PCC) Module description for more information.

The Reply Generator Module generates and sets the primary characteristics of the Sum, Delta, and Omni RF signals. It contains the circuits that set the target signal level, the Sum/Omni ratio, the Delta/Sum ratio, and the Delta/Sum phase. Each of these functions is controlled by signals from the PCC Module. Refer to the Reply Generator Module description for more information.

Figure 36. MBTS System Block Diagram



Each Upconverter Module translates one of the three 70 MHz signals from the Reply Generator to 1090 MHz. Channel A, or Channel B, or BIT output signals are available from each Upconverter. Each Upconverter also has three front panel test ports, one at 70 MHz, and two at 1090 MHz. Refer to the Upconverter Module description for more information.

The Reference Source Module generates low noise 16 MHz reference signals and three phase equivalent 1020 MHz LO signals. The 16 MHz signals are used as a reference by the PLL circuits within the other modules. The LO signals, at +13 dBm, are routed to each of the three Upconverter Modules to convert the 70 MHz IF signals to 1090 MHz. Refer to the Reference Source Module description for more information.

The IDR Module receives and demodulates interrogation signals from the radar system. RF signals may be selected from either of the Sum Channel inputs (diplexed with the reply signals) or from either of the two dedicated rear panel interrogation inputs. Demodulated data, PAM and DPSK, is routed to the PCC Module and to front panel test ports. Refer to the Interrogation Demodulation Receiver (IDR) Module description for more information.

The BIT Module includes circuits to test the reply generation and interrogation demodulation processes. It also measures the status of other system parameters such as power supply voltage and operating temperature. Refer to the Built In Test (BIT) Module description for more information.

3.2 Module Descriptions

3.2.1 Reply Generator

The Reply Generator Module produces three 70 MHz Intermediate Frequency (IF) target reply signals: Sum; Delta; and, Omni. The Process Control and Communications (PCC) Module controls the amplitude and phase relationship of these signals to simulate ATCRBS and Mode S target replies. The 70 MHz output signals from this module feed the three separate, but identical, Upconverter Modules (Sum, Delta, and Omni), in which the signals are converted to 1090 MHz target reply signals.

Figure 37. Reply Generator Front and Rear Views

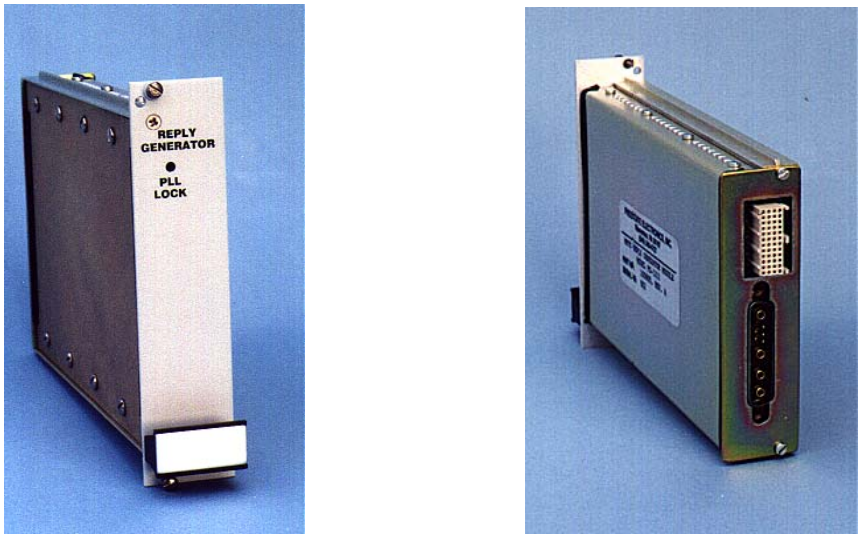


Figure 38. Reply Generator Block Diagram

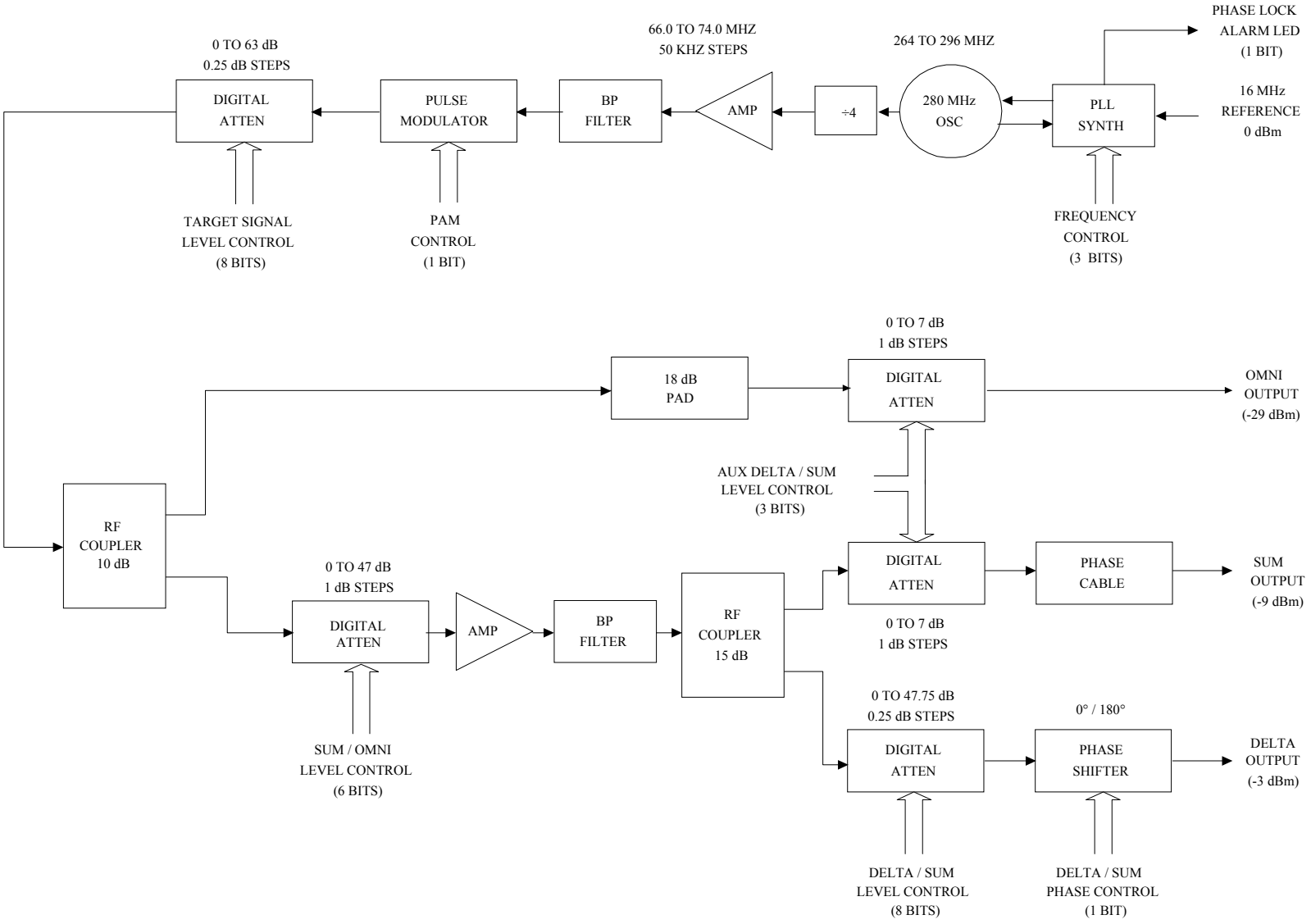


Figure 38, the Reply Generator Module Block Diagram, illustrates the signal processing circuits within the Reply Generator Module. These are described in the following paragraphs.

Signals within the Reply Generator Module derive from a Voltage Controlled Oscillator that is phase locked to a low noise, temperature stable signal from the Reference Source Module. The operating frequency of the oscillator is controlled by data inputs from the Process Control and Communications Module. The oscillator output signal frequency may be set anywhere from 264 to 296 MHz with a resolution of 200 kHz.

A sample of the VCO output signal is routed to a surface mount PLL Synthesizer IC. This IC divides the VCO signal by a fixed ratio (set by data inputs from the PCC Module) to a frequency of 200 kHz. The 16 MHz reference signal is also divided by a fixed ratio to a frequency of 200 kHz. Phase comparison of the two divided signals takes place and a DC error signal is generated. Loop characteristics, such as response time, reference side band levels, loop bandwidth, and stability factors, are set by low pass filter components in the DC feedback path. The VCO phase lock status is monitored and is indicated on an LED visible through the module front panel.

The VCO output signal (264 to 296 MHz) is coupled into a high-speed ECL divider IC that reduces the frequency of the input signal by a factor of four. It significantly improves the spectral response of the resultant70 MHz signal and also provides a high degree of isolation between the VCO and the PAM switching circuits. The frequency of the divider output signal ranges from 66 to 74 MHz (50 kHz step size).

A transimpedance amplifier boosts the level of the signal from the divider circuit to approximately +10 dBm. The amplifier's high input impedance does not load the divider output circuits. The amplifier's very low output impedance (through a 51 Ohm terminating resistor) provides an excellent signal match to the input of the following 70 MHz bandpass filter.

The three section 70 MHz bandpass filter greatly reduces all high frequency signal energy, such as harmonics from the preceding amplifier section and residual 280 MHz signals from the VCO. The filter has a 1 dB bandwidth of 26 MHz and an insertion loss of 1 dB.

The filtered 70 MHz signal is routed to the Pulse Modulator circuit. This circuit is comprised of two surface mount SPST terminating GaAs switches. The rise and fall times of the RF pulses out of the modulator are controlled, with 100 nanoseconds being typical of both characteristics. Each switch individually has in excess of 60 dB of Input to Output isolation at 70 MHz. The use of two switches, along with a careful PCB layout, achieves the specified On/Off ratio of 85 dB (typically 95 dB). One control signal activates both switches simultaneously.

The level of the amplitude modulated IF signal is set within the Target Signal Level digital attenuator. Three commercially available GaAs attenuator integrated circuits and two SPDT GaAs switch IC's perform this function. One IC has individual attenuator settings of 0.5, 1, 2, 4, 8, and 16 dB. A supplementary IC provides an additional 32 dB attenuator setting. The two GaAs switch IC's, along with discrete components, implement a 0.25 dB attenuation step. Thus, the total available attenuation range spans 0 dB to 63 dB in 0.25 dB step increments (an additional 32 dB of target level signal control is found in each Upconverter Module). Nine TTL control signals set the Target Signal Level attenuation value.

After passing through the target level control, the test signal is split into two signal paths by an RF coupler. The lower level signal from the coupler forms

the Omni (Ω) output of the Reply Generator Module. After passing through a fixed 18 dB attenuator and a variable 7 dB digital attenuator (normally set to 0 dB), the Omni signal exits the module at a level of –29 dBm. The variable 7 dB attenuator, the Auxiliary Delta/Sum Level Control, maintains a constant Sum/Omni signal ratio when Delta/Sum signal ratios greater than 6 dB are selected. Three TTL control signals are required to set the Aux Delta/Sum attenuation value. The higher level signal from the RF coupler is used to form the Sum (Σ) and Delta (Δ) signals within the Reply Generator.

The main signal from the RF coupler is connected to the Sum/Omni Level Control attenuator circuits. This function is accomplished through the use of a single GaAs attenuator integrated circuit. This IC provides signal attenuation in 1 dB increments from 0 to 63 dB. The total specified attenuation range of the Sum/Omni Attenuator is 0 dB to 47 dB with 1 dB step increments. Six TTL control signals are required to set the Sum/Omni attenuation value.

Signals from the Sum/Omni attenuator section are amplified by a wideband MMIC amplifier with a gain of 20.5 dB. A 70 MHz bandpass filter reduces signal harmonics created in the amplifier by at least 30 dB. Signals at the filter output are at a maximum level of +12.5 dBm.

The filtered IF signal is routed to a 10 dB coupler. The signal from the coupled output port traverses to the input of a 7 dB variable digital attenuator, the second half of the Aux Delta/Sum Level attenuator. The output of the attenuator connects to the Reply Generator Module Sum Output port through a phase-matching cable. The phase-matching cable is cut to a length (roughly 14 inches), which matches the phase of the Sum output signal to that of the Delta output signal. The exact length of the phase-matching cable is determined through test. The Sum signal exits the Reply Generator Module at a maximum level of -9 dBm.

Signals from the low loss output of the 10 dB coupler are routed to the Delta/Sum Level Control attenuator. At the input of Delta/Sum attenuator the maximum signal level is +11 dBm.

The Delta/Sum Level Control is used to simulate the notch amplitude response typical of the Delta channel in a Monopulse radar. It is comprised of three attenuator sections that provide a total amplitude adjustment range of 47.75 dB in increments of 0.25 dB. The Delta/Sum Attenuator is formed from two GaAs digital attenuator ICs, one switch control IC, two SPDT GaAs switches, and a number of discrete components. The two GaAs switches route the 70 MHz signal between either a 0 dB attenuation path or a 0.25 dB attenuation path. The 0.25 dB attenuator is implemented with precision discrete resistors. Signal attenuation in increments of 0.5 dB, 1 dB, 4 dB, 8 dB, and 16 dB is handled in one GaAs attenuator. The final 16 dB of signal attenuation occurs in the second attenuator. The maximum Delta signal level at the attenuator output is -2 dBm. Signal attenuation levels are set by real time inputs (8 bits) from the PCC Module.

The Delta/Sum signal phase relationship is set in a 0º/180º phase modulator hybrid circuit. Phase shift accuracy of the modulator circuit is better than 1º. Control of the modulator is through a single real-time TTL input from the PCC Module.

The maximum signal level at the Delta Output of the Reply Generator Module is -3 dBm.

3.2.2 Upconverter Module

The three RF outputs (Omni, Sum, and Difference) of the Reply Generator are cabled into three identical Upconverter Modules, one for each signal type. Within each Upconverter Module the signal from the Reply Generator is translated up to the output frequency, 1090 MHz, by the use of a 1020 MHz LO signal generated in the Reference Source Module. The 1090 MHz signal is filtered and switched through either an amplifier or an attenuator before being connected to the selected output channel. Since the frequency translation LO signals are phase equivalent and because the RF signal paths through the three Upconverter Modules are identical, the amplitude and phase relationships between each trio of Omni, Sum, and Difference signals (as generated in the Reply Generator Module) are maintained. Output channel selection, signal level control, and output signal presence are computer controlled from the PCC Module.

Figure 39. Upconverter Front and Rear Views

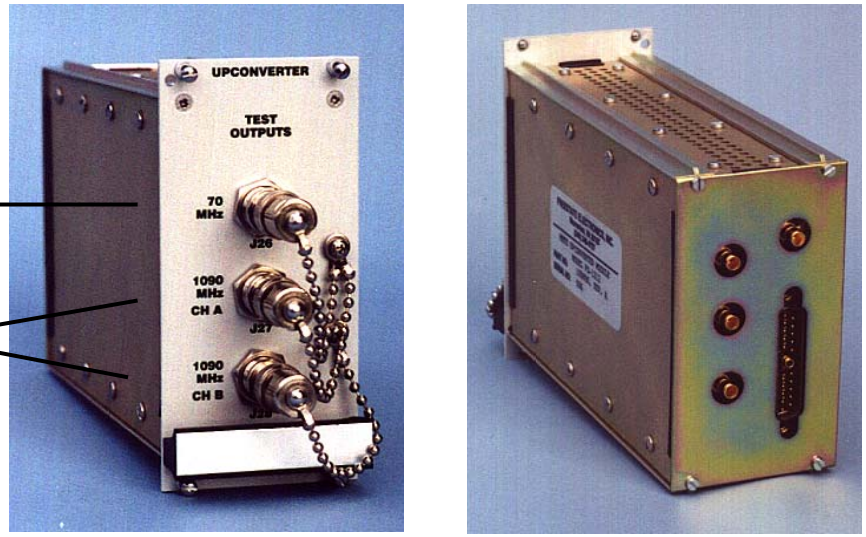


Figure 40. Upconverter Block Diagram

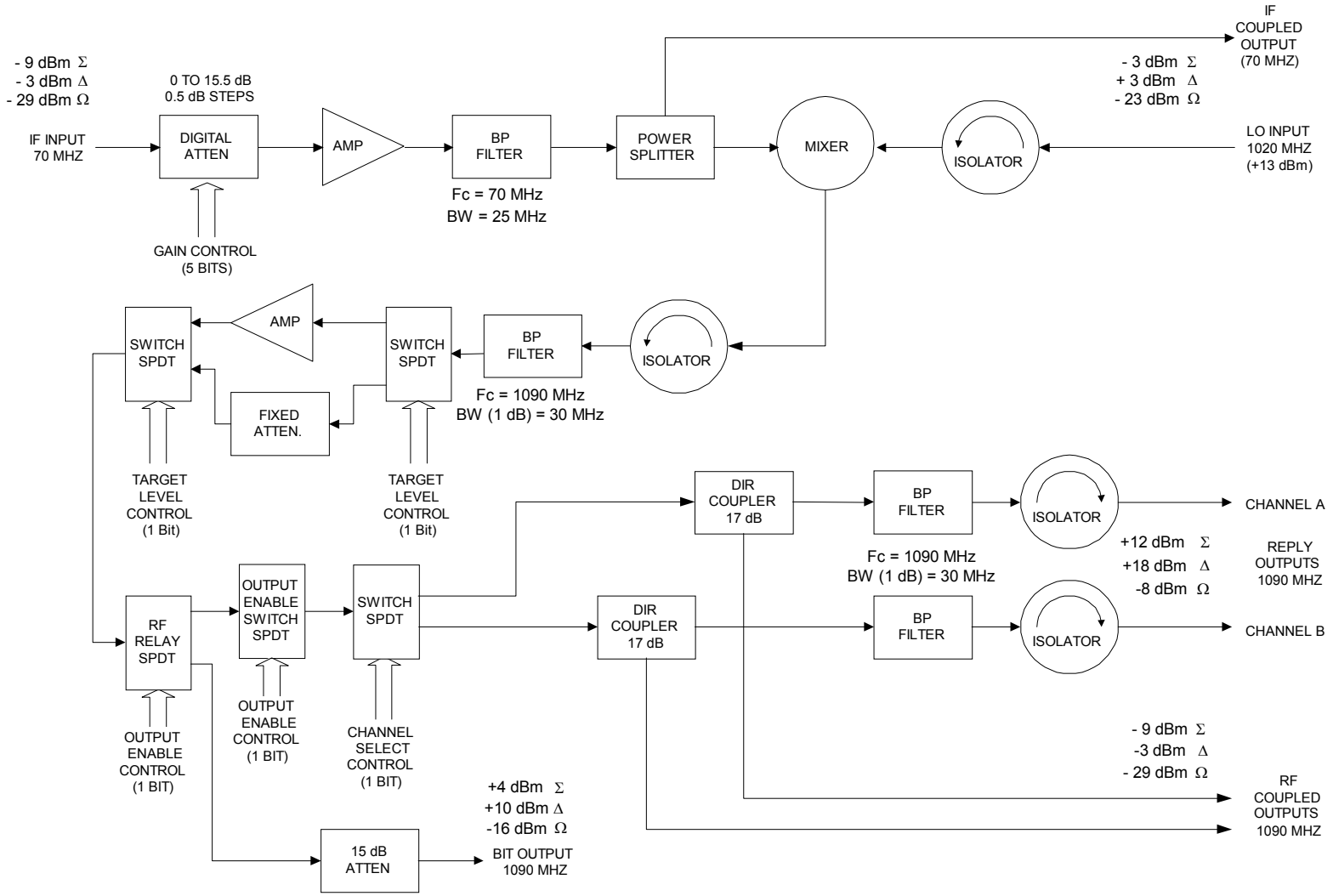


Figure 40, the Upconverter Module Block Diagram, illustrates the signal processing circuits within the Upconverter Module. These circuits are described in the following paragraphs. The three Upconverter Modules in each MBTS chassis have identical electrical and mechanical characteristics.

The 70 MHz signals from the Reply Generator are routed to a digitally controlled GaAs MMIC attenuator. This attenuator allows independent gain adjustment of the three Upconverter signals paths, so that signal levels external to the MBTS unit may be calibrated to meet system requirements. The signal level adjustment range is from 0 dB to 15.5 dB, in increments of 0.5 dB. Signals from the gain control attenuator are connected to the input of a precision hybrid amplifier that has a signal gain of 20 dB.

A five section 70 MHz bandpass filter eliminates signal harmonics that are produced in the hybrid amplifier. The filter has a 1 dB bandwidth of 25 MHz and at 140 MHz (the signal second harmonic) provides 50 dB of signal rejection. These properties of the filter allow the pulse amplitude modulated signals from the Reply Generator to pass through the filter without affecting the characteristics of the RF pulse. At the output of the filter the maximum Delta channel signal level is approximately +9 dBm.

The filtered 70 MHz signals are then routed to a 2-way power splitter. One signal from the splitter is connected to the IF Coupled Output connector. Signals at this port are cabled to the 70 MHz Test Output connector located on the front panel of the Upconverter Module. The 70 MHz Test Output is terminated with a 50 Ohm load so that the gain and phase properties of the RF signals in the MBTS unit are maintained. The nominal maximum Delta channel signal level at the test output is +3 dBm (Omni @ -23 dBm; Sum @ -3 dBm).

Signals from the second output of the power splitter are converted to 1090 MHz by an RF mixer. This high level, double balanced mixer exhibits excellent signal

conversion properties for the given input and output frequencies. Nominal signal conversion loss is 7.5 dB. At the mixer output port the nominal maximum Delta channel signal level is -4.5 dBm.

The +13 dBm, 1020 MHz conversion LO signal (generated in the Reference Source Module) passes through an isolator before entering the mixer. This isolator provides a good impedance match for the LO port of mixer U1, and also provides sufficient reverse isolation through the LO signal path to maintain the phase and amplitude integrity of the Omni, Sum, and Delta signal channels.

The spectrum of the output signal from the mixer contains not only the desired 1090 MHz signal but also high level signals at 1020 MHz, the LO signal, and at 950 MHz, the image product of the conversion process. The LO signal exits the mixer at a level of about -10 dBm. The image signal is at a power level that is equal to that of the 1090 MHz signal. Three (two in each signal channel) four-section, 1090 MHz bandpass filters reduce both undesired signals by at least 90 dB. The second filter also eliminates signal harmonics generated in the amplifier section that precede it. These filters have a 3 dB bandwidth of 30 MHz and an insertion loss of 1.5 dB.

The 1090 MHz signal at the output of the first filter connects to a RF switch network. The network sends the RF signal through either a linear amplifier with a nominal gain of 21 dB, or an attenuator with a nominal attenuation of 11 dB. The attenuator value is set to achieve a total change in RF gain of exactly 32 dB when the signal path switches.

The output of the switched RF section feeds a second linear amplifier with a gain of 10 dB. At the output of this amplifier, the maximum signal level is +24.5 dBm. The amplified 1090 MHz signal is then connected into a high isolation, normally open RF relay.

The RF relay insures that no signals exit the MBTS until set to do so by commands from the PCC Module. Input to output switch isolation is greater than 85 dB. A GaAs switch on the output of the relay adds an additional 40dB of RF input to output isolation. When the relay and switch are activated, signal energy passes from the relay output to the channel select switch.

The channel select network routes the output signal to either the Channel A or the Channel B signal line. This switch network is comprised of four GaAs MMIC switches. A high degree of isolation (85 dB) between the switch output ports is achieved through the use of multiple switch devices, considerable RF shielding, and control line filtering. Selection of the operational output channel is by a TTL input from the PCC Module. Delta channel signals at the selected switch output port are at a maximum level of +21 dBm (Sum @ +15 dBm, Omni @ -5 dBm).

Directional couplers in each output signal line direct a portion of the main output signal to the RF Coupled Output connectors. The 1090 MHz test outputs are located at the front panel of the Upconverter Module. Delta channel signals at either the Channel A or the Channel B Test Output are at a maximum level of -3 dBm (Sum @ -9 dBm, Omni @ -29 dBm).

Each high level signal from the directional coupler passes through a 1090 MHz bandpass filter and an isolator before exiting the module. The isolator is required to protect the preceding output circuitry from the high level (to +47 dBm peak power) interrogation radar pulses that may be present at the Sum or Omni output signal lines. The isolator provides more than 20 dB of reverse isolation. Forward insertion loss is in the order of 1 dB. At the module output, the maximum Delta channel signal level is +18 dBm (Sum @ +12dBm, Omni @ -8 dBm).

3.2.3 Interrogation Demodulation Receiver (IDR)

The Interrogation Demodulation Receiver Module selects a 1030 MHz signal from one of the MBTS Rear Panel connectors, either the Channel A input (J7), the Channel B input (J8), the Sum Channel A input (J1), the Sum Channel B input (J4), or the BIT Channel input and translates it down to an IF of 60 MHz. PAM and DPSK output data is then generated from the 60 MHz IF signal. These data outputs are routed to the PCC Module for further processing.

Figure 41. IDR Module Front and Rear Views

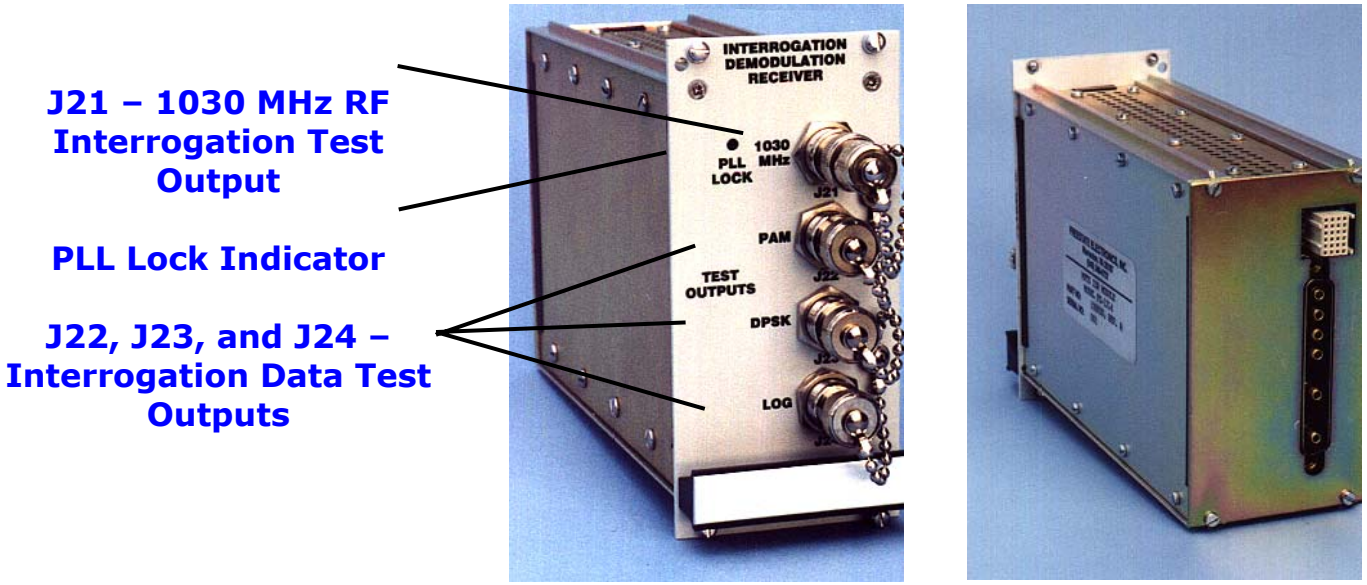


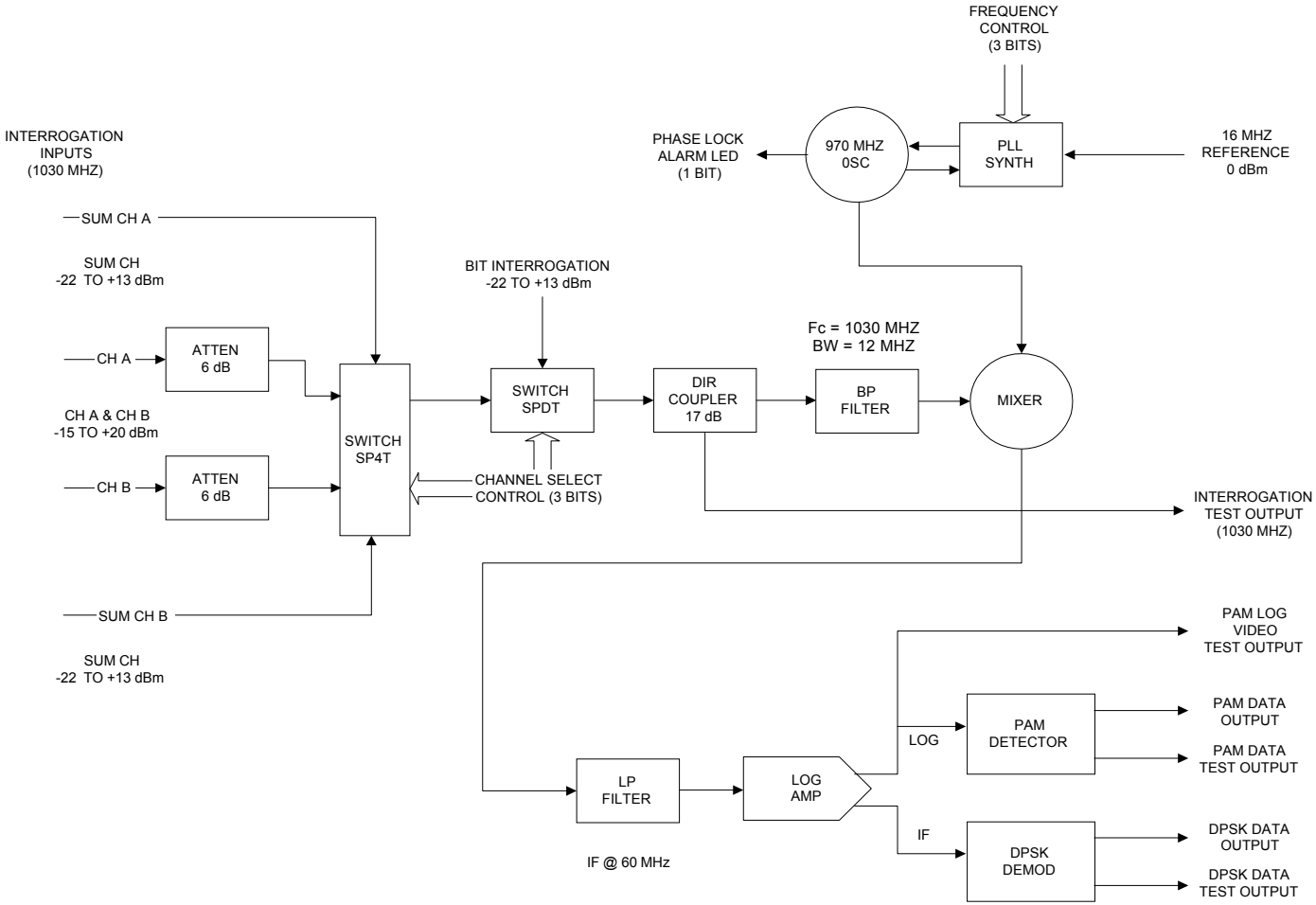
Figure 42, the IDR Module Block Diagram, illustrates the signal processing circuits within the IDR Module. These circuits are described in the following paragraphs.

1030 MHz interrogation signals can enter the IDR Module through five possible signal paths. These are the Channel A signal port, the Channel B signal port, the Sum Channel A signal port, the Sum Channel B signal port, and the BIT port. Signals from the Channel A and the Channel B inputs are routed through attenuators before reaching a SP4T channel selection switch. Both Sum Channel signals connect directly to this switch. BIT input signals are selected after the SP4T switch network.

The SP4T switch network connects one of the four input signal channels to the RF signal processing section of the module. The switch network is comprised of five GaAs MMIC switches. Port-to-port isolation of up to 85 dB is achieved through the use of multiple switch devices, RF shielding, and control line filtering. Selection of the operational input channel, or the BIT signal, is controlled by TTL inputs from the PCC Module.

The selected signal from the switch network then passes through an RF coupler to a five-section 1030 MHz bandpass filter. The signal from the coupled output port is cabled to a front panel connector for signal monitoring purposes. Signal levels at the test port range from -40 to -5 dBm. The bandpass filter in the main signal line permits only the interrogation signal to pass and be demodulated. The filter also keeps the conversion LO signal (at 970 MHz) from traversing back to the input connections of the module. The filter has a 1 dB bandwidth of 35 MHz. Rejection at 970 MHz and 1090 MHz is 40 dB and 80 dB, respectively. The filtered 1030 MHz energy is then routed to a high level mixer for conversion to 60 MHz.

Figure 42. IDR Module Block Diagram



Signal conversion to 60 MHz is accomplished by mixing the 1030 MHz signal energy with a 970 MHz LO signal generated within the IDR Module. Signal conversion loss through the mixer is approximately 7.5 dB. At the mixer output the 60 MHz interrogation signal is at a power level of between -40 dBm and -5 dBm.

The 970 MHz LO signal is derived from a voltage controlled oscillator that is phase locked to a low noise and temperature stable signal from the Reference Source Module. The operating frequency of the oscillator is controlled by data inputs from the Process Control and Communications Module. The output signal frequency is fixed at 970 MHz. The signal output level is +10 dBm.

A sample of the VCO signal is routed to a surface mount PLL Synthesizer IC. This IC divides the VCO signal by a fixed ratio (set by data inputs from the PCC Module) to a frequency of 200 kHz. The 16 MHz reference signal is also divided by a fixed ratio to a frequency of 200 kHz. Phase comparison of the two divided signals takes place and a DC error signal is generated. Loop characteristics, such as response time, reference side band levels, loop bandwidth, and stability factors, are set by low pass filter components in the DC feedback path to the voltage control input of the VCO. The VCO phase lock status is monitored and is indicated on an LED visible through the module front panel. Phase lock status is also sent to the PCC Module for monitoring.

The 60 MHz signal from the mixer passes through a 100 MHz low pass filter to a high accuracy log amplifier. The low pass filter eliminates the higher frequency mixer components (at 970 MHz and 1030 MHz) from the 60 MHz signal spectrum. The log amplifier generates detected log video and compressed IF output signals.

The output of the log IC exhibits a linear change in DC level based upon the logarithm of the power level of the input signal. A -15 dBm signal at the module input produces a 1.4 VDC response at the IC output, a +20 dBm signal produces yields a DC response of approximately 2 Volts. Circuit response times are more than fast enough to faithfully reproduce the amplitude characteristics of the pulsed interrogation input signal. The raw log video signal is cabled through a buffer amp to the PAM Test Output located on the RFTSS front panel. The raw log video signal, in conjunction with a fast comparator also generates TTL level PAM data pulses. A threshold adjustment suppresses output pulse generation when signals are below minimum specified input levels. The PAM data pulses are routed through a line driver to the PCC Module and to an IDR Module front panel test port.

The 60 MHz compressed IF output signal from the log amplifier IC is at a fixed level of approximately 0 dBm. This signal exits the log amplifier and passes through a SAW differential delay filter. This filter creates two equal amplitude, but differentially delayed in time, output signals. One output signal takes 250 nanoseconds longer to transition through the filter than the other. Signals from both filter outputs, at approximately -33 dBm, are amplified (with a gain of 18 dB) and then pass through variable delay lines. The variable delay lines adjust the differential delay between the two signals to exactly 250 nanoseconds.

The properly timed 60 MHz IF signals are amplified once again (with a gain of 32 dB), and then routed to an active mixer operating as a phase detector. Because the two signals have the proper time (and therefore phase) orientation demodulation of the DPSK encoded portion of the interrogation signal takes place. When the two demodulator input signals are in phase, a positive DC offset is produced at the IC output. When the

two input signals are 180º out of phase, a negative DC offset is produced at the IC output. The phase detector output, DC pulses at the data rate of the encoded DPSK signal, passes through a low pass filter circuit before reaching the input of a fast voltage comparator. The lowpass filter eliminates the 60 MHz frequency components from the DC signal. The filtered DC pulse signal is then converted to TTL levels in the voltage comparator. The DPSK data output signal passes through a line driver IC to the PCC Module and to an IDR Module front panel test port.

3.2.4 Reference Source

The Reference Source Module generates a stable, low noise 16 MHz reference signal that is used to phase locked all other MBTS oscillators. The Reference Source Module also generates three phase stable 1020 MHz LO signals for use in each of the three Upconverter Modules. Finally, the Reference Source generates a fixed frequency 1060 MHz signal used for calibration and alignment of the MSSR.

Figure 43. Reference Source Module Front and Rear Views

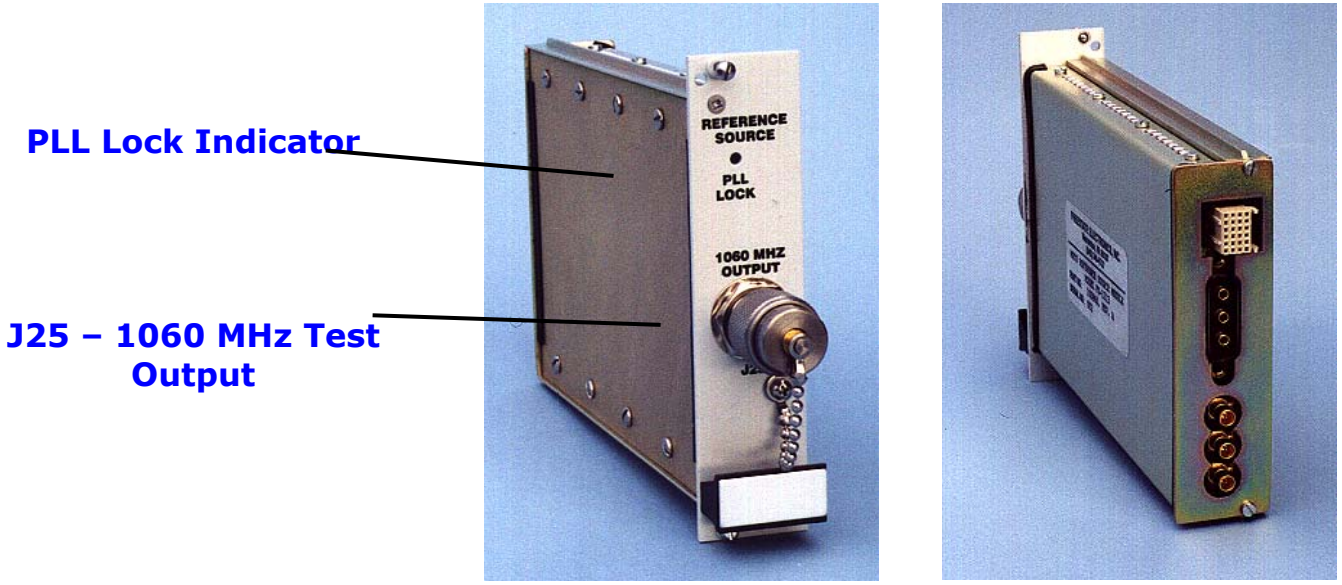


Figure 44, the Reference Source Module Block Diagram illustrates the signal processing circuits within the Reference Source Module. These circuits are described in the following paragraphs.

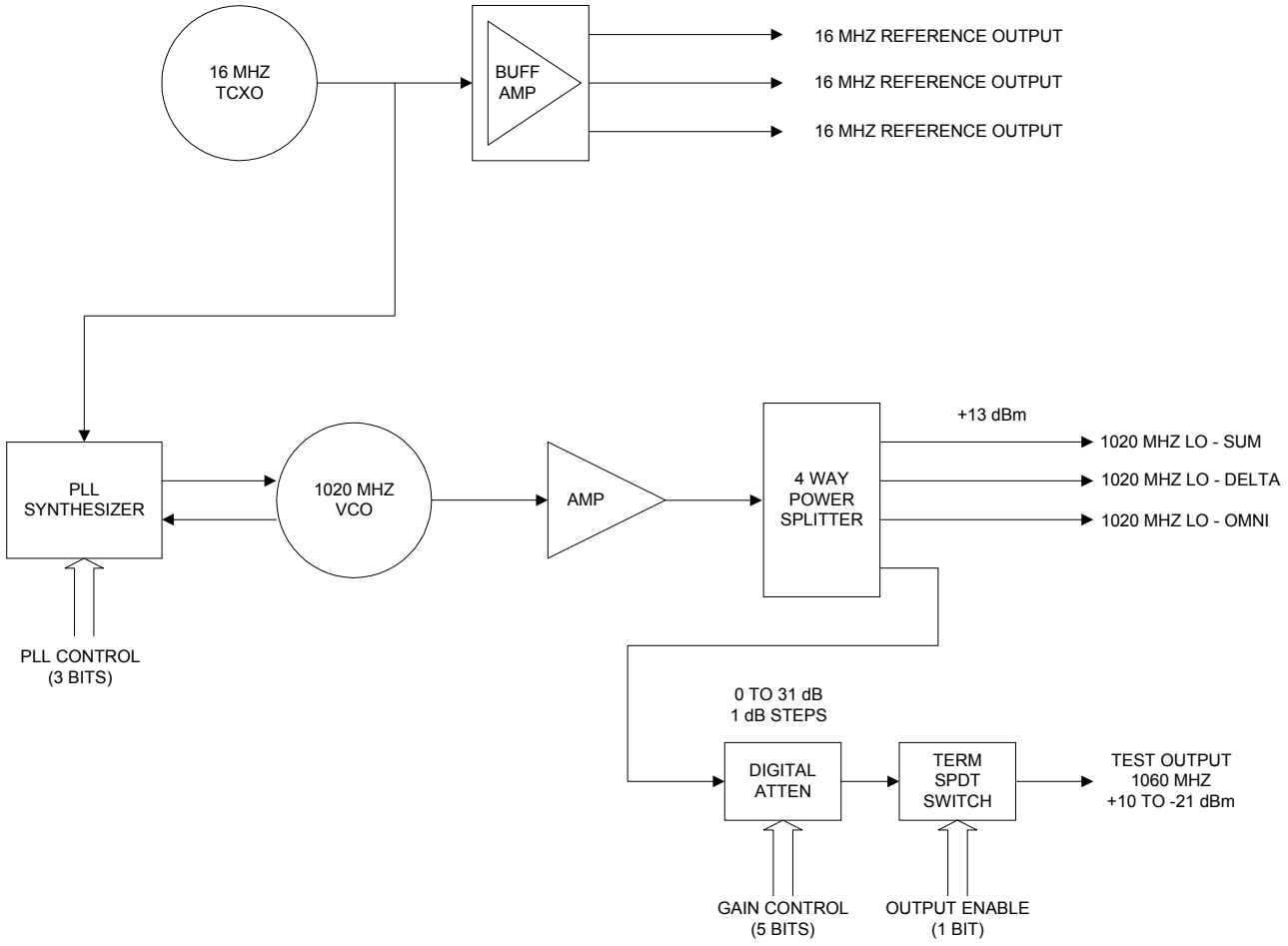
A temperature compensated crystal oscillator produces a low noise, +8 dBm, 16 MHz reference signal. This signal is routed to a buffer amplifier IC that provides three, +3 dBm, 16 MHz reference signals to the module output connections.

The 1020 MHz LO signal is derived from a VCO that is phase locked to the 16 MHz reference signal. The operating frequency of the oscillator is controlled by data inputs from the Process Control and Communications Module. The output signal frequency is normally fixed at 1020 MHz. However, as the output frequency of the MBTS is varied from 1080 MHz and 1100 MHz, the LO signals tunes over a frequency range of 1010 MHz to 1030 MHz (in 200 kHz step increments). Also, the operator may desire to enable the 1060 MHz CW Test Output function. The VCO frequency is then changed to 1060 MHz (and all Reply outputs from the Upconverter Modules are disabled).

The VCO output signal is generated within a high quality, surface mount, hybrid oscillator assembly. The signal output level is +12 dBm. Typical phase noise at a 10 kHz offset is -90 dBc/Hz.

A portion of the VCO output signal is routed to a surface mount PLL Synthesizer IC. This IC divides the VCO signal by a fixed ratio (set by data inputs from the PCC Module) to a frequency of 200 kHz. The 16 MHz reference signal is also divided by a fixed ratio to a frequency of 200 kHz. Phase comparison of the two divided signals takes place and a DC error signal is generated. Loop characteristics, such as response time, reference side band levels, loop bandwidth, and stability factors, are set by low pass filter components in the DC feedback path. The VCO phase lock status is monitored and is indicated on an LED visible through the module front panel.

Figure 44. Reference Source Module Block Diagram



The phase stable 1020 MHz signal from the VCO is amplified to a level of +20 dBm. The signal from the amplifier output is then directed to a four-way power splitter. The outputs of the splitter, four equal amplitude (+13 dBm) LO signals, are routed to the Omni, Sum, and Difference module output ports, and through a digitally controlled GaAs MMIC attenuator and RF switch to the 1060 MHz Test Output. Phase equivalence of the Sum and Difference LO signals is maintained through precise control of the circuit trace geometry on the PCB.

The GaAs MMIC attenuator permits operator control of the 1060 MHz Test Output signal level. The attenuator IC has 31 dB of control range with a resolution of 1 dB. At the 1060 MHz Test Output signal amplitude may be set between +10 dBm to -21 dBm.

A high isolation terminating GaAs RF switch selectively enables or disables the presence of RF energy at the 1060 MHz Test Output port. Input to output switch isolation is greater than 45 dB. The 1060 MHz Test Output port is located at the module front panel. Signal connection is through an N style connector.

3.2.5 Built In Test (BIT)

The BIT Module verifies the basic performance of the MBTS. The module consists of an Interrogator section, a Level Detector and Phase Demodulator section, and a Microcontroller section. The Interrogator section generates ATCRBS and Mode S interrogation signals that verify the performance of the demodulation circuits in the IDR Module. The Level Detector section verifies the amplitude and phase performance of all reply output signals generated by the Reply Generator and Upconverter Modules. The Microcontroller section controls both of these processes through the generation of timed digital test stimuli in response to commands communicated from the PCC Module.

Figure 45. Built In Test Module Front and Rear Views

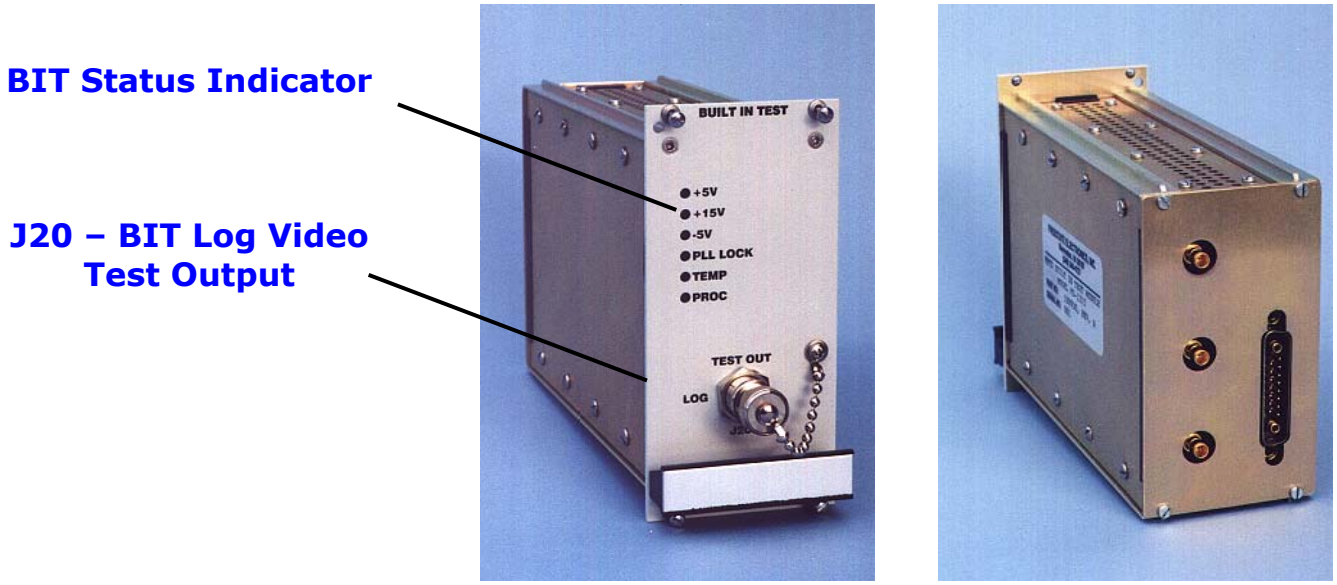


Figure 46. BIT RF Block Diagram

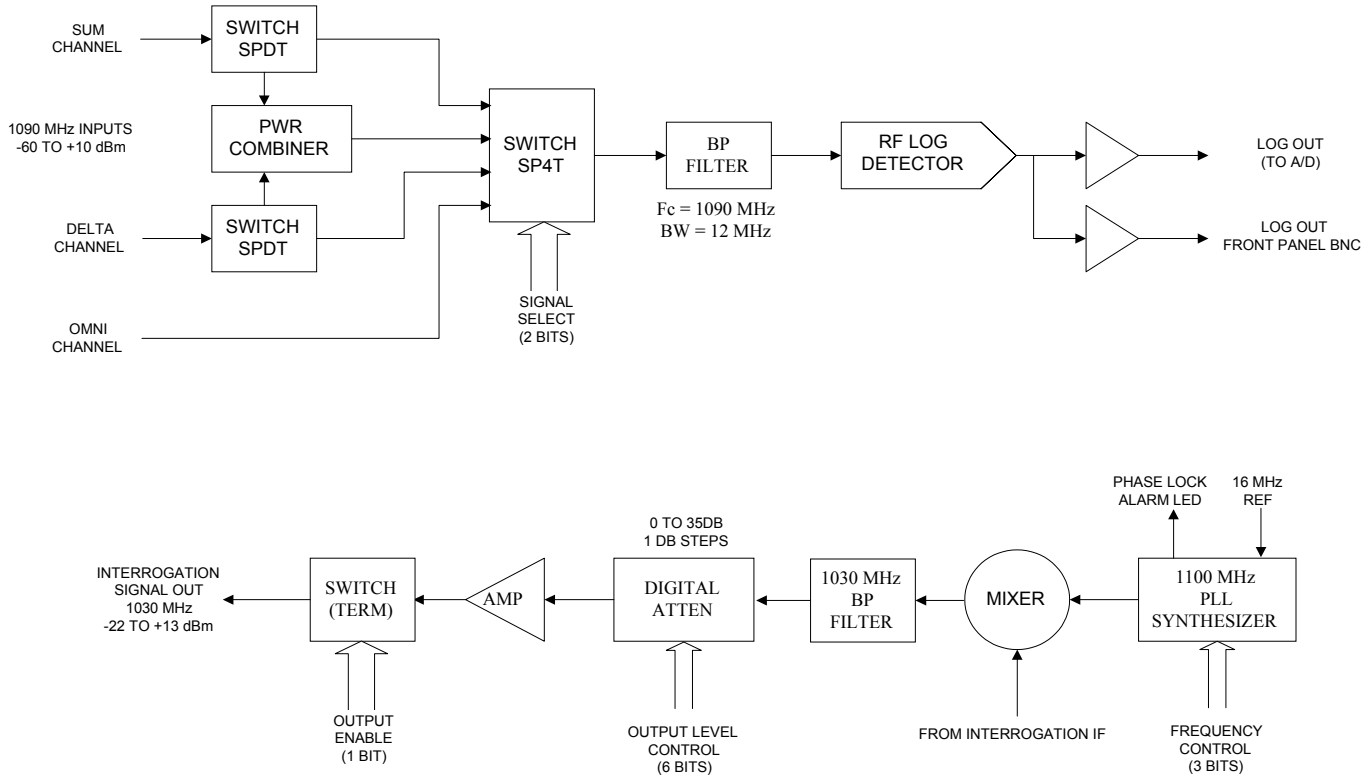
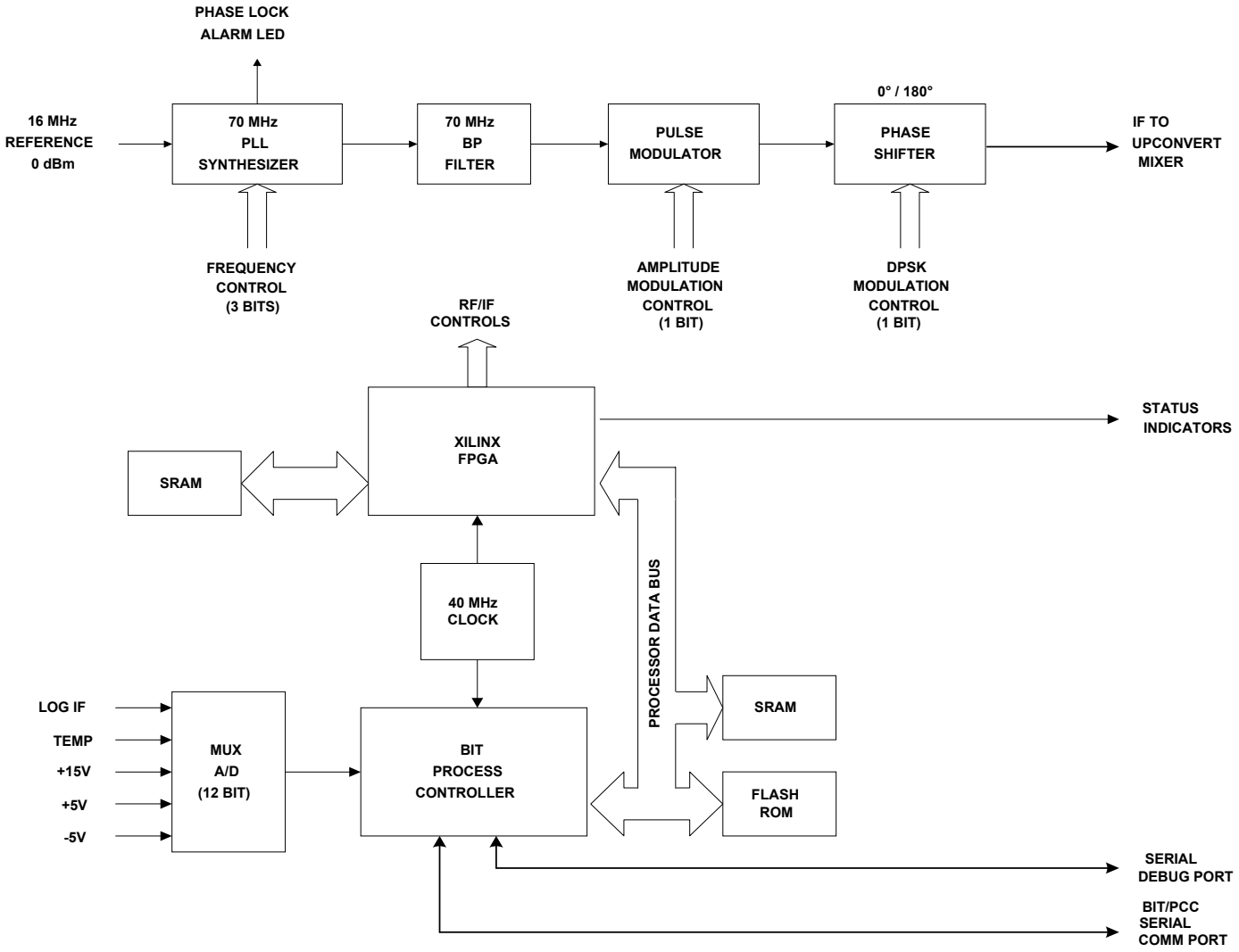


Figure 47. BIT Processor and IF Block Diagram



BIT measurements are performed when the MBTS powers up and upon operator request. BIT Module interrogation signals are generated through the use of a set of stored modulation data sequences. The data sequences when applied to the RF modulating circuits form ATCRBS type 2, 3/A, B, and C, plus Mode S Roll-Call and All-Call test interrogation patterns. Pulse timing, width, duration, or other pulse parameters are not operator controllable features. Data received by the Process Control and Communications Module from the IDR Module is evaluated against expected received data patterns for errors. A BER of greater than 1×10^{-4} causes a fault condition and generates a MBTS service request.

The Level Detector section of the BIT Module verifies the operation of all processor controlled reply generation circuits. The Reply Generator is set to operate in CW mode. The BIT Module makes signal strength measurements as each Reply Generator and Upconverter attenuator or phase control bit is toggled. The measurements are compared against predetermined pass/fail criteria. Unexpected or improper signal operation results in a fault condition and generates a MBTS service request.

The BIT Module measures and monitors the three DC power supply voltages (+15V, +5V, and -5V) and the air temperature internal to the chassis. The DC voltages and the voltage from the temperature monitor IC are multiplexed with the detected RF signal input at the input to the A/D Converter. The operational status of all monitored signals is communicated to the PCC Module. Other specified BIT functionality, such as PLL status, azimuth status, etc., is handled by the microcontroller within the PCC Module.

Figure 46, the BIT RF Block Diagram, and Figure 47, the BIT Processor and IF Block Diagram illustrate the signal processing circuits within the BIT Module. These circuits are described in the following paragraphs.

3.2.5.1 BIT Interrogator

Interrogation signals within the BIT Module derive from the 70 MHz PLL Synthesizer. The primary components of this circuit are a PLL loop comprised of a voltage controlled oscillator and a synthesizer IC. The VCO is phase locked to the low noise, temperature stable, signal from the Reference Source Module. The operating frequency of the oscillator is controlled by data inputs from the BIT Microcontroller. The normal VCO frequency is 280 MHz, which ultimately produces an output signal at 1030 MHz. The VCO frequency may be set anywhere from 264 to 296 MHz with a resolution of 200 kHz.

The VCO signal is generated within a high quality, surface mount, hybrid oscillator assembly. The signal output level is +10 dBm. Typical phase noise is -110 dBc/Hz at a 10 kHz offset.

A portion of the VCO output signal is routed to the surface mount PLL Synthesizer IC. This IC divides the VCO signal by a fixed ratio (set by data inputs from the microcontroller) to a frequency of 200 kHz. The 16 MHz reference signal is also divided by a fixed ratio to a frequency of 200 kHz. Phase comparison of the two divided signals takes place and a DC error signal is generated. Loop characteristics, such as response time, reference side band levels, loop bandwidth, and stability factors, are set by low pass filter components in the DC feedback path. The VCO phase lock status is monitored and is indicated on an LED visible through the module front panel.

The VCO output signal (280 MHz) is coupled into a high-speed ECL divider IC that reduces the frequency of the input signal by a factor of four. The frequency of the divider output signal is 70 MHz. A transimpedance amplifier boosts the level of the signal from the divider circuit to

+5.5 dBm. The amplifier provides an excellent signal match to the input of the following 70 MHz bandpass filter.

The three section 70 MHz bandpass filter greatly reduces all high frequency signal energy, such as harmonics from the preceding amplifier section or residual 280 MHz signal from the VCO. The filter has a 1 dB bandwidth of 26 MHz and an insertion loss of 1 dB.

The filtered 70 MHz signal enters the Pulse Amplitude Modulator circuit at a level of +4.5 dBm. The PAM circuit is comprised of a terminating GaAs MMIC switch and a switch driver IC. Switch off state isolation is greater than 50 dB. Pulse amplitude modulated RF signals are created with the application of pulsed control signals from the BIT microcontroller.

When Mode S interrogations are created the 70 MHz signal is also DPSK modulated. This is accomplished through the use of a 0º/180º phase modulator circuit and properly timed modulation control signals. Phase shift accuracy of phase modulator is better than 1º. Signal insertion loss through the modulator is about 1 dB. The DPSK modulated 70 MHz signal is at a level of approximately -5 dBm.

The modulated 70 MHz signal is converted to 1030 MHz in the Interrogation mixer. The mixer exhibits excellent signal conversion properties at the given input and output frequencies. Nominal mixer signal conversion loss is 7.5 dB. At the mixer output port the level of the desired signal is approximately -12.5 dBm.

The 1100 MHz conversion LO signal is derived from the 1100 MHz PLL Synthesizer section. The primary components of this circuit are a PLL loop comprised of a voltage controlled oscillator and a synthesizer IC. The voltage controlled oscillator (VCO) is phase locked to the low noise reference source signal. The microcontroller circuit within the BIT Module

sets the operating frequency of the oscillator. The LO signal frequency is fixed at 1100 MHz. The design characteristics of this synthesizer section are similar to those of the 70 MHz synthesizer.

The spectrum of output signals from the mixer contains not only the desired 1030 MHz signal but also high level signals at 1100 MHz, the LO signal, and at 1170 MHz, the image product of the conversion process. The LO signal exits the mixer at a level of about -10 dBm. The image signal is at a power level that equals that of the desired 1030 MHz signal. A five-section 1030 MHz bandpass filter reduces both of these extraneous signals by 50 dB. This filter has a 3 dB bandwidth of 30 MHz and an insertion loss of 1.5 dB.

After filtering, a GaAs MMIC digital attenuator sets the interrogation output signal level. This attenuator is set to an attenuation value of between 3 dB and 38 dB. At the attenuator output the signal level varies between -17 dBm and -52 dBm. For most BIT operations, the BIT Microcontroller automatically sets the value of signal attenuation.

The 1030 MHz signal at the attenuator output connects to the input of a pair of cascaded amplifiers. These two linear amplifiers boost the RF signal by a total of 33.5 dB, to a maximum level of +16 dBm. The amplified signal then passes through a terminating SPDT GaAs FET switch to the module output. The switch enables or disables signal presence at the module output connector. Switch isolation is greater than 45 dB. When the switch is enabled, the level of the 1030 MHz signal at the BIT Module Interrogation Signal Output varies from –22 dBm to +13 dBm.

3.2.5.2 BIT Level Detector

The BIT Level Detector selects the 1090 MHz signal to be measured from one of three RF input ports. Signals at these ports derive from the BIT outputs of the Sum, Delta, and Omni Upconverter Modules. The selected signal is routed to a precision, monolithic log amplifier that measures the level of the RF signal. The DC signal from the log amplifier IC is digitized in a 12-bit A/D converter. The A/D data outputs are then routed to the onboard microcontroller for analysis or transfer to the PCC Module.

A network of SPDT and SP4T GaAs FET switches, controlled by the BIT microcontroller, selects the RF signal to be processed. The performance of the Reply Generator phase modulator is verified by combining the Sum and Delta signals. The power level of the combined signals is then measured as the phase modulator is switched from a 0º state to a 180º state. A change in power level equivalent to a minimum of 20 dB is expected.

The selected RF signal is routed to a four-section 1090 MHz bandpass filter. The filter permits only the 1090 MHz Reply signal to pass and be detected. The log amplifier generates an accurate and repeatable DC signal that corresponds to the power level of the selected 1090 MHz signal. The log amp output is linear for logarithmic (dB) changes in the applied RF signal power level. The DC signal from the log detector is connected through buffer amps to a 12-bit A/D converter.

The A/D converter has eight multiplexed input signal lines, of which five are used. The A/D circuit measures the DC signal from the RF log detector, the voltage from a temperature measurement IC, and the three DC power supply voltages (+15V, +5V, and –5V). The A/D conversion process is controlled by the BIT microcontroller. The converter accommodates an input signal range of 0 to 5 Volts. This yields a LSB

conversion resolution of 1.22 mV, which is 4 to 5 times finer than what is required to resolve a 0.25 dB change in any of the RF signals. Data from the A/D is routed to the microcontroller and then communicated to the PCC Module for analysis. Verification of the performance of each RF amplitude and phase control is accomplished by the measurement of detected RF signal levels, routed into the BIT Module from each Upconverter Module, as they are individually set by the PCC Module.

3.2.5.3 BIT Microcontroller

The BIT Microcontroller section interfaces with the PCC Module to control all of the BIT functions. BIT functions include control and monitoring of the BIT RF hardware, the generation of RF test interrogation pulses, verification of the operation of all amplitude and phase controls in the reply signal path, temperature monitoring, temperature compensation measurement of reply signal power levels, and monitoring of power supply voltages.

The core processor components consist of an Intel 80C188EB processor, static RAM and FLASH ROM. A Xilinx FPGA provides the interface between the processor and the BIT RF hardware. The A/D converter measures detected RF signal levels, power supply voltages, and BIT Module ambient temperature. Front panel LEDs display the operational condition of the power supply voltages, module temperature, PLL lock, and of the microprocessor. Overall BIT status is displayed on the PCC Module front panel.

Memory includes both RAM and Flash ROM. RAM is static and is configured as an array of 128K words of 8 bits each (128 Kbytes). Flash ROM is configured as an array of 512K words of 8 bits each (512 Kbytes).

The Flash ROM may be written to by the CPU to save firmware and FPGA downloads through the serial (RS-232) communications port.

The timing and sequencing of PAM and DPSK interrogation modulation data is controlled by the FPGA. The modulating interrogation data information is contained in the FPGA RAM buffer. The contents of this buffer are loaded by the microcontroller from one of the seven possible interrogation patterns (six fixed, one user programmable) stored in the Flash ROM. Two bits are stored for every interrogation time sample – one sets the PAM output state and the second sets the DPSK phase state. The buffer contents are clocked out at a rate set by the FPGA modulation clock, converted into serial data, and then sent to the modulation circuits in the RF section. BIT interrogations are generated a single sequence at a time in response to commands received from the PCC Module.

The BIT Module communicates with the PCC Module via a CMOS asynchronous serial port. This serial port uses the same data format as an RS-232 port. For almost all BIT functions, the BIT Module is a slave to the PCC Module (i.e. the BIT Module never initiates any tests). The exceptions are temperature and power supply monitoring. The BIT Module monitors these conditions continuously, though it reports their status to the PCC only when requested. A listing of the full PCC Module to BIT Module commands is provided in the PCC/BIT Module Command Set (FSE Document No. 100682).

The BIT Module also provides a CPU remote RS-232 debug port. This interface allows access to built-in debugging features of the processor. It is used for factory maintenance and repair only.

3.2.6 Process Control and Communications (PCC)

The primary functions of the PCC Module include:

- Interpretation and analysis of ATCRBS and Mode S radar interrogation signals
- Generation of signals to control the timing and amplitude characteristics of simulated transponder reply responses
- Performance verification of all MBTS interrogation/reply systems through the implementation of Built In Test functions
- Support of operator functions and settings communicated to the MBTS from the Operator Control System (OCS) via an IEEE-488 interface

Figure 48. PCC Module Front and Rear Views

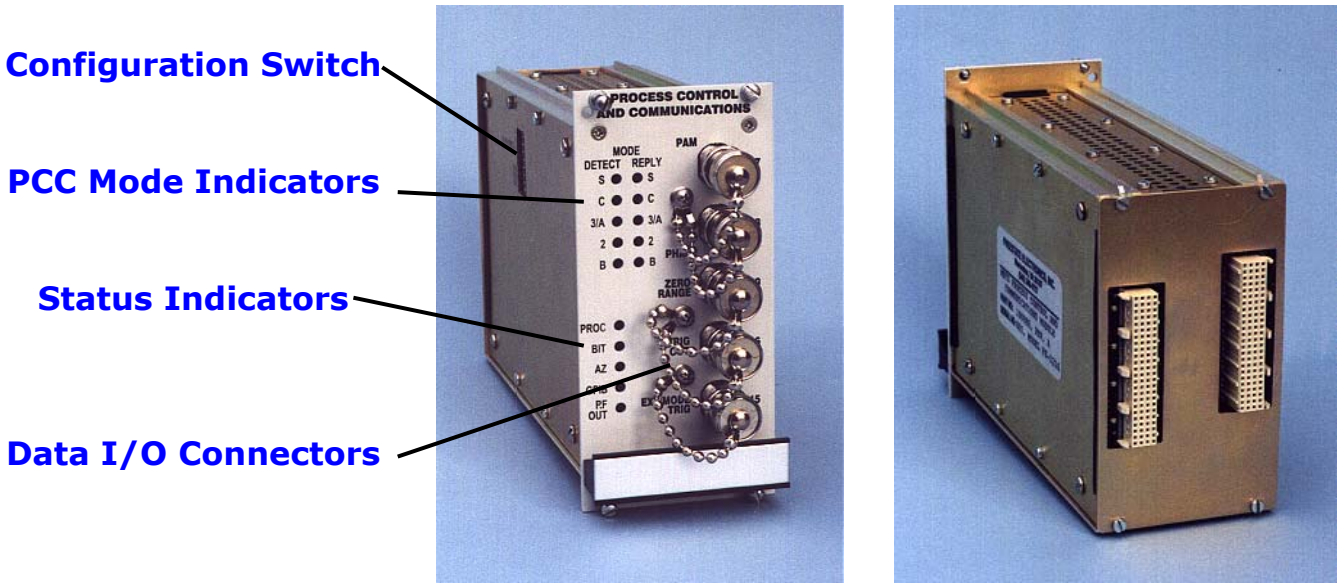
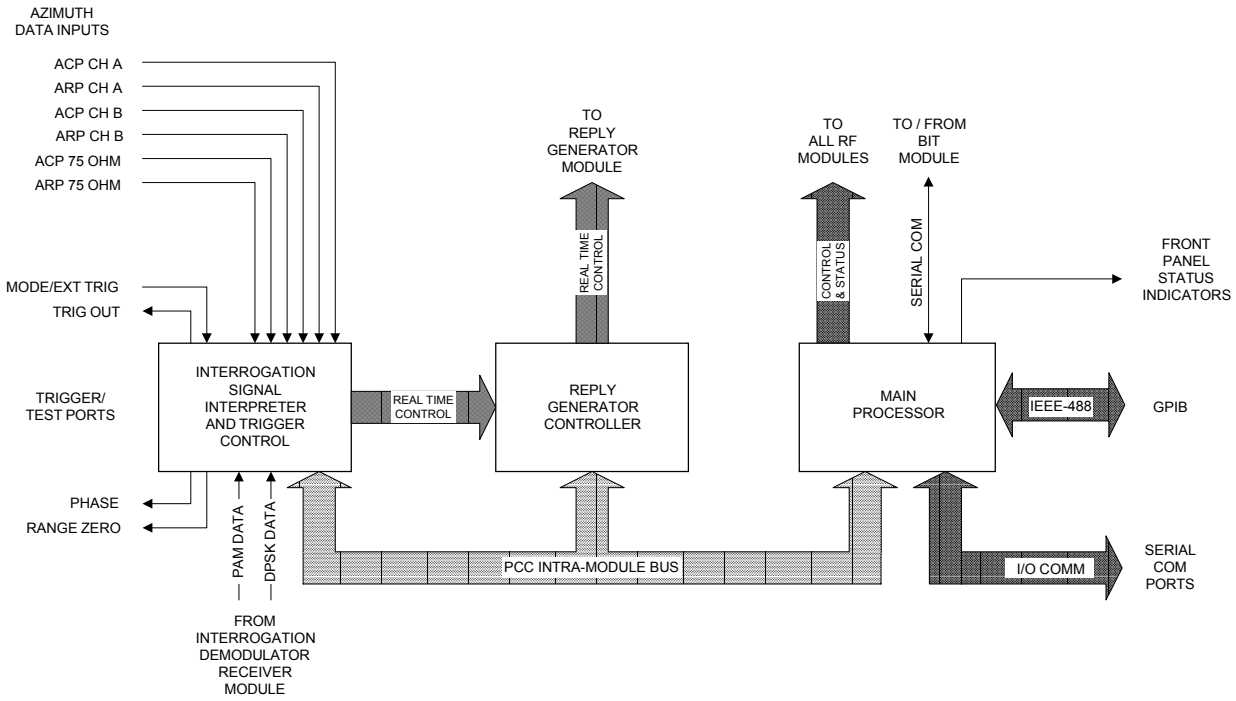


Figure 49. PCC Module Block Diagram



3.2.6.1 PCC Module Overview

The PCC Module performs real-time and non real-time functions. Real-time functions include the analysis of interrogation data and the generation of target replies. Non real-time functions include control and monitoring of MBTS operating frequencies, signal levels, input and output channel selections, BIT functionality, and handling of either GPIB or serial communications. An intra-module data bus passes non real-time setup and status information between each of the internal processing sections of the PCC Module.

The PCC Module is comprised of three functional component blocks: the PCC Main CPU (CPU), the Interrogation Signal Interpreter and Trigger Control (ISI), and the Reply Generator Controller (RGC). Figure 49, the PCC Module Block Diagram, indicates the primary connections into the PCC Module and the major signal connections between the three functional blocks that make up the PCC Module.

The ISI and the RGC, located on one of two printed circuit board assemblies inside the PCC Module, perform all of the real-time processing functions that are required to generate simulated target responses. This includes interpretation of azimuth data from the antenna, the verification of the demodulated PAM and DPSK interrogation data, and the calculation and generation of all RF control signals that determine the characteristics of the simulated aircraft transponder response. Two Xilinx FPGA devices perform almost all ISI and RGC processes.

The CPU, located on a second printed circuit board, serves as the central control element for the PCC. It is comprised of an Intel model 80C188EB processor, Flash ROM and RAM memory, remote control ports, and an

MBTS Inter-Module Interface that communicates with and sets the operating parameters of each of the other MBTS modules.

The 80C188EB is a 16-bit microprocessor that operates at a clock rate of 40 MHz. It combines fifteen to twenty of the most common microprocessor components onto one chip and is object code compatible with the 8086/8088 microprocessors. Memory includes both RAM and Flash ROM. RAM is static and is configured as an array of 128K words of 8 bits each (128 Kbytes). Flash ROM is configured as an array of 512K words of 8 bits each (512 Kbytes). The Flash ROM may be written to by the CPU to save firmware and FPGA updates from the RS-232 Control Port. An intra-module data bus passes non real-time setup and status information between each of the three functional components.

A dedicated IEEE-488 ASIC provides the GPIB communications interface between external devices and the CPU microprocessor. All GPIB communications through this interface follow the transmission protocols listed in the IEEE-488.2 specification. The MBTS IEEE-488 Command Set (FSE Document No. 100681) lists the commands, responses, and data formats that are required for proper communication with and control of the MBTS and the PCC Module. The IEEE-488 port is the means by which the OCS communicates with the MBTS.

Two serial communication ports provide an interface between the PCC CPU and external communication devices. Both ports follow the protocols and guidelines established in the ANSI RS-232C specification. One port is used to upload firmware and FPGA updates and may also be used as a secondary means of controlling the MBTS. The second RS-232 port provides access to the built-in debug features of the 80C188EB processor. This port is not accessible through any connectors on the exterior of the MBTS.

A third serial communication port provides an interface between the PCC CPU and the microprocessor located within the BIT Module. The PCC CPU is the system controller of this interface. The command set and data format applicable to this interface are listed in the PCC/BIT Module Command Set (FSE Document No. 100682).

A Xilinx FPGA implements the functions of the MBTS Inter-Module Interface. The use of this device permits unlimited reprogramming cycles to implement in-circuit functional upgrades and design modifications.

3.2.6.2 IEEE-488 Control

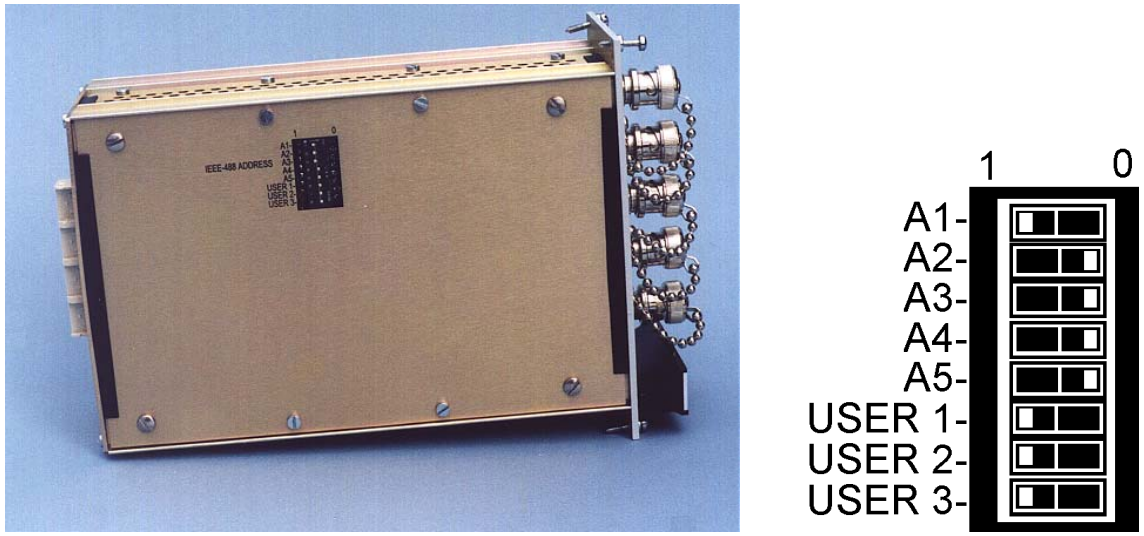
An IEEE-488 port (rear panel J12 – IEEE-488 Connector) provides a communication interface between external GPIB devices and the PCC CPU microprocessor. All GPIB communications through this interface follow the transmission protocols listed in the IEEE-488.2 specification. The MBTS IEEE-488 Command Set (FSE Document No. 100681) lists the commands, responses, and data formats that are required for proper communication with and control of the MBTS and the PCC Module. A Configuration Switch sets the PCC IEEE-488 bus address. The configuration switch is accessed through a cut-out in the side cover of the PCC Module chassis.

3.2.6.2.1 PCC IEEE-488 Address Configuration and Calibration Setup

The PCC module uses an 8-position Configuration Switch, accessible through the module side cover, to set the GPIB bus address (see Figure 50).

IEEE-488 ADDRESS SWITCH. Switch A1 denotes the Least Significant Bit (LSB), and A5 denotes the Most Significant Bit (MSB) of the GPIB address switch. Bit weighting is 1, 2, 4, 8, and 16 respectively for switch controls A1 through A5. The MBTS is delivered with a default address 1 (see Figure 50).

Figure 50. PCC Module Side View Showing Setup Switches and Detail



Switches A1 through A5 are used for setting the IEEE-488 bus address to a binary value between decimal 0 and 31. User 1 enables/disables overwriting factory calibration settings. User 2 and User 3 are for factory use only.

USER SWITCH 1. When switch USER 1 is set to Position 1 overwriting of the internal calibration tables and factors is prevented. When set to position 0, any of the calibration tables internal to the MBTS can be erased or overwritten.

USER SWITCH 2 and 3. Switches USER 2 and USER 3 are for special factory procedures only. For normal MBTS operation these should remain in position 0. Both switches need to be set to Position 1 to enable the use of software and firmware field upgrades.

CAUTION

Keep the USER 1 switch set to position 1 to prevent overwriting of factory set calibration tables and factors.

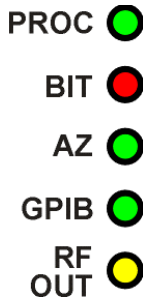
3.2.6.3 RS-232 Control

An RS-232 communication port (J13 – Auxiliary RS-232 Control Port) located on the rear panel of the MBTS provides a serial interface between the PCC CPU and external communication devices. Communications through this port follow the protocols and guidelines established in the ANSI RS-232C specification.

3.2.6.4 Status Indicators

The PCC front panel, Figure 48, has five LED status indicators as shown in Figure 51. A green LED indicates that the function is operationally active and working properly. A yellow LED indicates that the function is either inactive or in an indeterminate state. A red LED indicates that the function is in a failure mode.

Figure 51. PCC Status Indicators



PROC LED. The PROC LED indicates the status of monitored processor functions within the PCC Module. This LED normally flashes green once a second.

BIT LED. The BIT LED indicates the status of monitored BIT functions such as internal temperature, power supply voltages, memory integrity, etc.

AZ LED. The AZ LED indicates the status of APG signals from the selected APG input channel. The LED turns red if no APG signals are detected or if they do not meet specification requirements. If the Antenna Alarm function is disabled the AZ LED will always be green.

GPIB LED. The GPIB LED indicates the status of communications over the IEEE-488 interface. The LED is green when the interface is active.

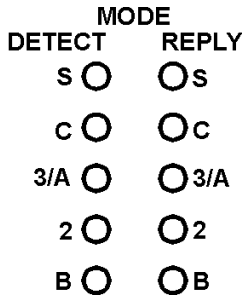
RF OUT LED. The RF OUT LED is green when one of the primary RF output channels of the MBTS, either channel A or B, is selected for use. The RF OUT LED is yellow when the BIT signal path, internal to the MBTS, is

selected. Refer to the Output Select section for more information on selected an active output channel.

3.2.6.5 Mode Indicators

The PCC Module includes two rows of MODE indicators as shown in Figure 52.

Figure 52. PCC Mode Indicators



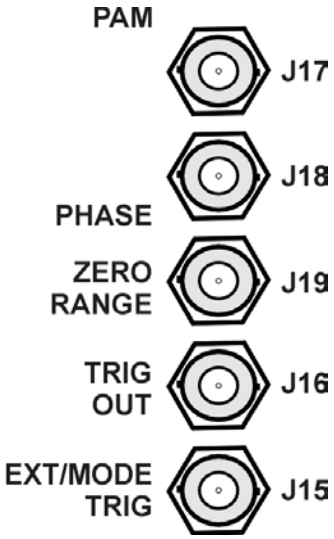
MODE DETECT INDICATORS. The five MODE DETECT LED indicators display the trigger signal types detected by the MBTS. Each valid trigger signal detected by the PCC will result in the momentary illumination of its associated MODE DETECT LED. The trigger type is automatically determined when either RF interrogation or Mode Pair triggers are used. When either external or internal pulse triggers are used, the 1060 MHz CW Mode control assigns a trigger type to the trigger signal. If trigger signals are applied at a rate of greater than approximately 30 per second the LED will appear to be a solid green. Two or more indicators may appear to be simultaneously illuminated if interleaved interrogation sequences are applied to the MBTS.

MODE REPLY INDICATORS. The five MODE REPLY LED indicators display the reply signal types generated by the MBTS. The Target Type control sets the type of reply signal the MBTS will generate for a given trigger signal. The association between trigger signal type and reply response type follows transponder requirements as stated in National Air Standard guidelines.

3.2.6.6 Data I/O Connectors

The PCC Module has five front panel connectors as shown in the figure below. Refer to Section 2.3.2.4.2, PCC Module Test Ports and Status Indicators, for a full description of the use of these test ports.

Figure 53. PCC Module Front Panel Connectors



J17 – PAM Reply Data

J18 – Phase Reply Data

J19 –Zero Range Data

J16 – Trigger Out

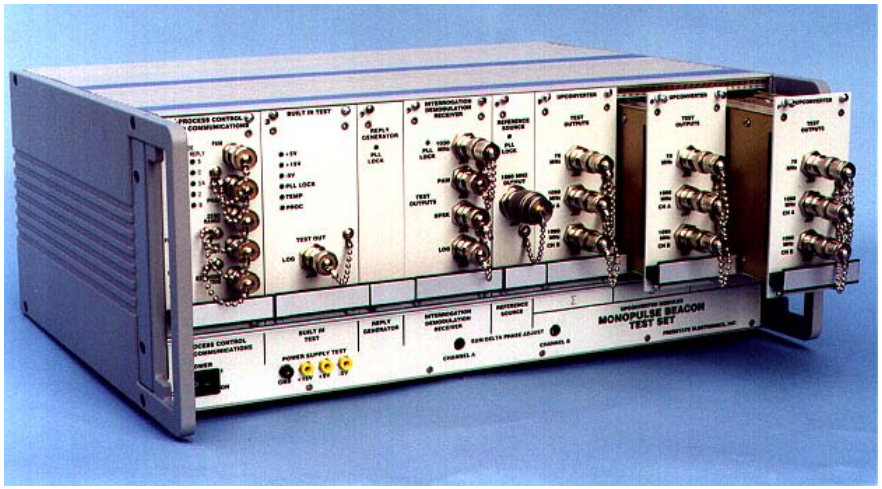
J15 – Mode/External Trigger

3.3 MBTS Chassis

3.3.1 Front Panel

As shown in Figure 54, the MBTS is comprised of eight removable modules in a 19-inch rack mount chassis. Each 6 HP wide module is attached to the chassis mainframe by a captive panel screw at the top and bottom of the module. Each 12 HP wide module is attached to the chassis by four captive panel screws, two on the top and two on the bottom. Each module can be easily removed by pulling on the module handle after the captive screws have been loosened. Figure 2 provides links to descriptions of all front panel controls and plug-in modules.

Figure 54. MBTS Front Panel with Modules Partially Removed



3.3.1.1 Power Switch

The MBTS AC power switch is located in the lower left corner of the front panel. The switch rocker positions are marked ON and OFF. When in the OFF position the mechanical rocker opens both the neutral and hot sides of the incoming AC line.

3.3.1.2 Power Supply Test Points

Power supply test points are located directly beneath the BIT Module. They provide a means to externally measure the output voltages of the internal power supplies. The black test point is connected to chassis ground. The three yellow test points are provided, one for each of the +15V, +5V, and -5V DC outputs.

For proper operation, the +5V output should be at +5±0.25 volts, the –5V output should be at –5±0.25 volts, and the +15V output should be at +15±0. 5 volts. The high impedance test points are designed only for voltage monitoring and cannot supply current for any operational purposes.

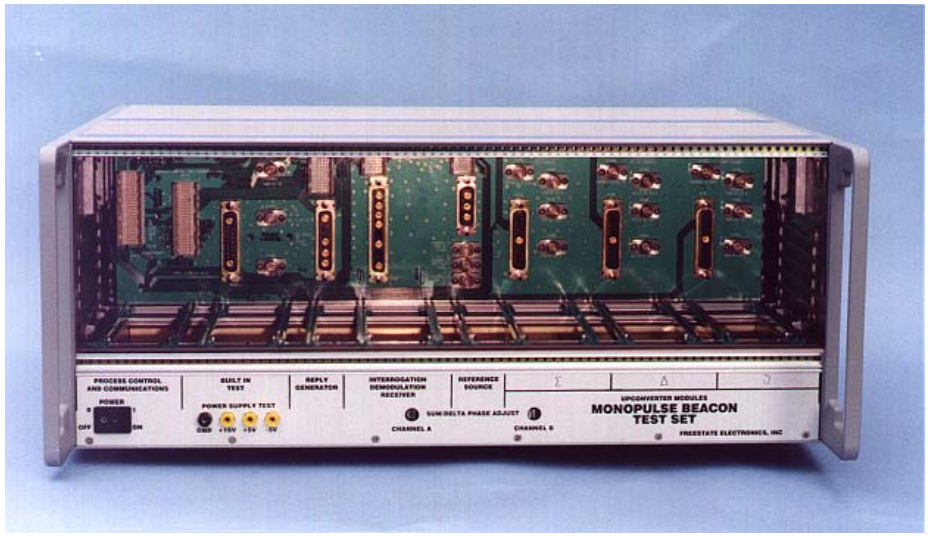
3.3.1.3 Sum/Delta Phase Adjust

Two precision phase adjustment devices, one for output Channel A and one for output Channel B, are accessible through the MBTS Front Panel. These devices match the phase of the Delta RF output signal to that of the SUM RF output. The phase adjusters are set at the factory to achieve the proper phase characteristics at the output of the MBTS. During system integration, adjustment of these may be required to match the phase characteristics of the MBTS to radar site requirements.

3.3.2 Chassis Internal Description

Figure 55 shows a view of the front of the MBTS with all modules removed. Each module fits into a specific chassis location. Module locations are labeled on the lower MBTS front panel. Guide rails align each module as it is inserted into its designated chassis slot. Blind-mate connectors, on each module and on the internal motherboard, provide a signal interface between all modules and rear panel connections. Refer to the MBTS Front Panel for module placement and location.

Figure 55. MBTS Chassis Front View with all Modules Removed



3.3.3 Chassis Cooling

A fan, internal to the MBTS, provides air circulation inside of the unit. Clearance above and below the unit is required for proper cooling. Never place objects on the MBTS that will restrict air flow through the unit.

When installed in an equipment rack, clearance of at least 1.75 inches above and below the chassis is recommended for proper cooling.

CAUTION

Always provide clearance above and below the MBTS when it is operating.

3.3.4 Rear Panel

Refer to Figure 3, MBTS Rear Panel, for links to descriptions of all signal interfaces found on the rear panel of the MBTS.

4 STANDARDS AND TOLERANCES

4.1 MBTS General Operating Characteristics

The MBTS mounts in a 7-inch (4U) high opening of a standard 19-inch rack or equipment cabinet. It is designed for indoor operation only. Table 2 lists the General Operating Characteristics of the MBTS.

Table 2. MBTS General Operating Characteristics

Characteristic	Specification
Weight	35 pounds
Size	Front Panel - 7 x 19 (H X W) inches Rear Panel - 7 x 17.625 (H x W) inches Depth - 14 inches
Power	115 to 230 VAC, 50-60 Hz, 60 Watts, typical
Temperature	Operating: +10°C to 50°C Storage: -20°C to +70°C
Relative Humidity	0% to 90%, non-condensing
Altitude	Operating: 10,000 feet Storage/Shipping: 20,000 feet
Shock and Vibration	Normal bench handling

4.2 MBTS Signal Interfaces

Signal interfaces are located on the rear and front panels of the MBTS. The primary interrogation and target reply signal connectors are located on the MBTS chassis rear panel. The 75 Ohm ACP and ARP azimuth inputs, the RS-422 ACP and ARP azimuth inputs, the IEEE-488 control, the RS-232 control, and the AC power input are also located on the chassis rear panel. Video, IF, and RF test inputs and outputs are located on the front panels of the various plug-in modules.

4.2.1 Rear Panel Signal Interfaces

Refer to Figure 3 for rear panel connector locations.

4.2.1.1 J1 through J6 - 1090 MHz Reply Outputs and Sum Channel Interrogation Inputs

The 1090 MHz Channel A and Channel B target reply output signal connectors are located on the MBTS rear panel. In some system configurations the Sum signal connectors, J1 and J4, also connect the 1030 MHz radar interrogation pulses into the MBTS. Type N female connectors are used in all cases. Connector reference designators are:

J1 - SUM Channel A Target Reply Output (and SUM Channel A Radar Interrogation Input)

J2 - DELTA Channel A Target Reply Output

J3 - OMNI Channel A Target Reply Output

J4 - SUM Channel B Target Reply Output (and SUM Channel B Radar Interrogation Input)

J5 - DELTA Channel B Target Reply Output

J6 - OMNI Channel B Target Reply Output

Table 3. J1 - SUM Channel A Target Reply Output (and SUM Channel A Radar Interrogation Input)

Connector Reference Designator	J1
Connector Name	1090 MHz Target Reply Output, Sum Channel A (and 1030 MHz Radar Interrogation Input, Sum Channel A)
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, 50 Ohms
Interrogation Input Level	+27 dBm to +47 dBm, peak, 1030 MHz
Reply Output Level	Adjustable, -85 dBm to +10 dBm
Output Signal Frequency	1090 MHz nominal, 1080 MHz to 1100 MHz, adjustable in 200 kHz increments

To: Section 4.2.1, Rear Panel

Table 4. J2 - DELTA Channel A Target Reply Output

Connector Reference Designator	J2
Connector Name	1090 MHz Target Reply Output, Delta Channel A
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, 50 Ohms
Input Level	Not Applicable
Reply Output Level	Adjustable, less than -110 dBm to +16 dBm
Signal Frequency	1090 MHz nominal, 1080 MHz to 1100 MHz, adjustable in 200 kHz increments

To: Section 4.2.1 Rear Panel

Table 5. J3 - OMNI Channel A Target Reply Output

Connector Reference Designator	J3
Connector Name	1090 MHz Target Reply Output, Omni Channel A
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, 50 Ohms
Input Level	Not Applicable
Reply Output Level	Adjustable, less than -100 dBm to -10 dBm
Signal Frequency	1090 MHz nominal, 1080 MHz to 1100 MHz, adjustable in 200 kHz increments

To: 4.2.1 Rear Panel

Table 6. J4 - SUM Channel B Target Reply Output (and SUM Channel B Radar Interrogation Input)

Connector Reference Designator	J4
Connector Name	1090 MHz Target Reply Output, Sum Channel B (and 1030 MHz Radar Interrogation Input, Sum Channel B)
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, 50 Ohms
Interrogation Input Level	+27 dBm to +47 dBm, peak, 1030 MHz
Reply Output Level	Adjustable, -85 dBm to +10 dBm
Signal Frequency	1090 MHz nominal, 1080 MHz to 1100 MHz, adjustable in 200 kHz increments

To: 4.2.1 Rear Panel

Table 7. J5 - DELTA Channel B Target Reply Output

Connector Reference Designator	J5
Connector Name	1090 MHz Target Reply Output, Delta Channel B
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, 50 Ohms
Input Level	Not Applicable
Reply Output Level	Adjustable, less than -110 dBm to +16 dBm
Signal Frequency	1090 MHz nominal, 1080 MHz to 1100 MHz, adjustable in 200 kHz increments

To: 4.2.1 Rear Panel

Table 8. J6 - OMNI Channel B Target Reply Output

Connector Reference Designator	J6
Connector Name	1090 MHz Target Reply Output, Omni Channel B
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, in/out, 50 Ohms
Input Level	Not Applicable
Reply Output Level	Adjustable, less than -100 dBm to -10 dBm
Signal Frequency	1090 MHz nominal, 1080 MHz to 1100 MHz, adjustable in 200 kHz increments

To: 4.2.1 Rear Panel

4.2.1.2 J7 and J8 - 1030 MHz Radar Interrogation Inputs

1030 MHz Channel A and Channel B radar interrogation signals can connect to the MBTS through rear panel connectors J7 and J8. Refer to Figure 3 for rear panel connector locations.

Table 9. J7 and J8 - Channel A and B Interrogation Inputs

Connector Designator Reference	J7 and J8
Connector Name	J7 - 1030 MHz Interrogation Input, Channel A J8 - 1030 MHz Interrogation Input, Channel B
Connector Location	MBTS Rear Panel
Connector Type	"N"
VSWR/Impedance	1.5:1 maximum, 50 Ohms
Interrogation Input Level	-15 dBm to +20 dBm, peak
Output Level	Not Applicable
Signal Frequency	1030 MHz, nominal

To: 4.2.1 Rear Panel

4.2.1.3 J9 - RS-422 Balanced APG Data Inputs

Balanced (RS-422) ACP and ARP azimuth data signals are connected into the MBTS through rear panel connector J9. Unbalanced (75 ohm) ACP and ARP data may also be connected into the MBTS (see Section 4.2.1.4).

Table 10. J9 – RS-422 Antenna Azimuth Data Inputs

Reference Designation	J9
Connector Name	RS-422 Antenna Azimuth Data Inputs
Connector Location	MBTS Rear Panel
Connector Type	DB-15 female
Data Format	Compatible with all standard radar system platforms
Pulse Frequency	ARP – 1 pulse every 4 to 15 seconds ACP – 4096 pulses per ARP IACP - 16384 pulses per ARP
Balanced Electrical Inputs	Conforms with all RS-422 specifications, 0.0 to 5.0 volts (differential)
Signals Connections	pins 1, 6, 7, 13, 14, and 15 – No Connection
	pin 2 – Channel A +ACP
	pin 3 – Channel B +ACP
	pin 4 – Channel A +ARP
	pin 5 – Channel B +ARP
	pin 8 – Signal Ground
	pin 9 – Channel A -ACP
	pin 10 – Channel B -ACP
	pin 11 – Channel A -ARP
	pin 12 – Channel B -ARP

4.2.1.4 J10 and J11 – 75 Ohm APG Data Inputs

Unbalanced (75 ohm) ACP and ARP data are connected into the MBTS through rear panel BNC connectors J10 (ACP input) and J11 (ARP input). Balanced (RS-422) ACP and ARP azimuth data signals may also be connected into the MBTS (see Section 4.2.1.3). Refer to Figure 3 for rear panel connector locations.

Table 11. J10 – 75 Ohm Azimuth ACP Input

Connector Reference Designator	J10
Connector Name	75 Ohm ACP Input
Connector Location	MBTS Rear Panel
Connector Type	BNC
VSWR/Impedance	75 Ohm
Input Level	TTL
Signal Frequency	Variable, 4096 or 16384 pulses per ARP (Antenna rotation rate within 4 to 15 RPM)

Table 12. J11 - 75 Ohm Azimuth ARP Input

Connector Reference Designator	J11
Connector Name	75 Ohm ARP Input
Connector Location	MBTS Rear Panel
Connector Type	BNC
VSWR/Impedance	75 Ohm
Input Level	TTL
Signal Frequency	Variable, 1 pulse per antenna revolution (Antenna rotation rate within 4 to 15 RPM)

4.2.1.5 J12 – IEEE-488 Connector

The IEEE-488 interface, J12, is located on the rear panel of the MBTS. All pin name and numbering assignments are per IEEE-488 standards as shown in Table 12. Refer to Figure 3 for rear panel connector locations.

Table 13. J12 - IEEE-488 Connector Pin Designations

Pin Number	Designation	Pin Number	Designation
pin 1 -	DIO1	pin 13 -	DIO5
pin 2 -	DIO2	pin 14 -	DIO6
pin 3 -	DIO3	pin 15 -	DIO7
pin 4 -	DIO4	pin 16 -	DIO8
pin 5 -	EIO	pin 17 -	REN
pin 6 -	DAV	pin 18 -	GND
pin 7 -	NRFD	pin 19 -	GND
pin 8 -	NDAC	pin 20 -	GND
pin 9 -	IFC	pin 21 -	GND
pin 10 -	SRQ	pin 22 -	GND
pin 11 -	ATN	pin 23 -	GND
pin 12 -	SHIELD	pin 24 -	LOGIC GND

4.2.1.6 J13 – Auxiliary RS-232 Control Port

The Auxiliary RS-232 serial communications interface, J13, is located on the rear panel of the MBTS. The serial interface conforms with the protocols listed in ANSI/TIA/EIA-232F. The Auxiliary RS-232 Control Port uses the same command structure as the IEEE-488 interface. The interface operates at 9600 baud, 8 data bits, 1 stop bit and no parity bit. Handshaking should be turned off. Refer to Figure 3 for rear panel connector locations.

Table 14. J13 – Auxiliary RS-232 Control Port

Connector Designator Reference	J13
Connector Name	Auxiliary RS-232 Control Port
Connector Location	MBTS Rear Panel
Connector Type	DB-9 Female
Signals	pin 2 - TX Data pin 3 - RX Data pin 5 - Ground

4.2.1.7 J14 – AC Power

AC power is applied to the MBTS through rear panel connector J14. Refer to Figure 3 for rear panel connector locations.

Table 15. J14 - AC Power Input Connector

Connector Reference Designator	J14
Connector Name	AC Power
Connector Location	MBTS Rear Panel
Connector Type	3 Prong IEC
Input Level	105 to 265 Volts AC
Maximum Current Draw	0.8 Amperes
Signal Frequency	50 to 60 Hz
Fuse Type	3AG Type, 1 Amp, 250 VAC

4.2.1.8 Fuse

The MBTS is protected from current overload by Fuse F1, which is a 3AG Type, rated at 1 Ampere, 250 VAC. The fuse holder is located on the MBTS rear panel.

4.2.2 Front Panel Connectors

4.2.2.1 J15 through J19 – Data Interfaces

There are five MBTS data signal interface connections. These include the Mode/External Trigger Input (J15), the Trigger Output (J16), the PAM Output (J17), the Phase Output (J18), and the Range Zero (J19) Outputs. These connections are located on the front panel of the Process Control and Communications (PCC) Module. All connectors are type BNC.

Refer to Figure 2 for the front panel module locations.

Refer also to Section 2.3.2.4.2, PCC Module Test Ports and Status Indicators, for a description of the use of these test ports.

Specifications for each of the connectors can be found in the following tables:

Table 16. J15 – Mode/External Trigger

Table 17. J16 – Trigger Out

Table 18. J17 – PAM Reply

Table 19. J18 – Phase Reply

Table 20. J19 –Zero Range Data

Table 16. J15 – Mode/External Trigger

Connector Name	Mode/External Trigger
Connector Reference Designator	J15
Connector Location	PCC Module Front Panel Connectors
Connector Type	BNC
Signal Description	Trigger signal input for target reply generation
VSWR/Impedance	75 Ohm
Input Level	TTL Compatible, Trigger occurs on rising edge of input pulse, or per ATCRBS Mode Pair specifications
Pulse Width/Timing	Pulse width = 0.1 μSec, minimum; ATCRBS Mode Pair specifications applicable to all Mode Pair trigger signals
Signal Frequency	Up to 3000 trigger signals per second

Table 17. J16 – Trigger Out

Connector Name	Trigger Out
Connector Reference Designator	J16
Connector Location	PCC Module Front Panel Connectors
Connector Type	BNC
Signal Description	Trigger output pulse created by MBTS in response to every valid trigger signal
VSWR/Impedance	75 Ohm
Output Level	TTL Compatible
Signal Frequency	At the rate of detected triggers, pulse width user variable from 0.1 to 5.0 μSec

Table 18. J17 – PAM Reply Data

Connector Name	PAM Reply Data
Connector Reference Designator	J17
Connector Location	PCC Module Front Panel Connectors
Connector Type	BNC
Signal Description	Pulse amplitude modulating sequence applied to target reply circuits of the MBTS
VSWR/Impedance	75 Ohm
Output Level	TTL Compatible, low enable
Pulse Width/Timing	Set by ATCRBS and Mode S data specifications, operator variable pulse width and pulse timing

Table 19. J18 – Phase Reply Data

Connector Name	Phase Reply Data
Connector Reference Designator	J18
Connector Location	PCC Module Front Panel Connectors
Connector Type	BNC
Signal Description	Phase modulating signal applied to the target reply circuits of the MBTS
VSWR/Impedance	75 Ohm
Input Level	Not Applicable
Output Level	TTL Compatible, TTL 1 = 0º Sum/Delta phase, TTL 0 = 180º Sum/Delta phase
Signal Frequency	Data rate dependent upon reply requirements

Table 20. J19 –Zero Range Data

Connector Name	Zero Range Data
Connector Reference Designator	J19
Connector Location	PCC Module Front Panel Connectors
Connector Type	BNC
Signal Description	Zero range marker of RF target reply signal, Target range delay begins coincident with this signal
VSWR/Impedance	75 Ohm
Input Level	Not Applicable
Output Level	TTL Compatible, rising edge indicates zero range of target reply
Signal Frequency	Data rate and signal timing dependent upon reply requirements

4.2.2.2 J20 – BIT Log Video Test Output

The signal level of the selected BIT RF input is monitored at the BIT LOG TEST OUT port, (J20). The connector is located on the front panel of the BIT Module. See Figure 45. When not in use this test port should be terminated with the attached 50 Ohm load.

Table 21. J20 – Log Video Test Output

Connector Name	Log Video Test Out
Connector Reference Designator	J20
Connector Location	BIT Module Front Panel
Connector Type	BNC
VSWR/Impedance	1.5:1, 50 Ohm
Output Level	Log video representation of the level of the selected RF signal (Omni, Sum, or Delta signal Channels), 0.6 Volts to 1.7 Volts into 50 Ohms
Signal Frequency	At the rate of BIT test pattern sequence

4.2.2.3 J21 – 1030 MHz RF Interrogation Test Output

The selected 1030 MHz interrogation signal (CH A, CH B, Sum CH A, Sum CH B, or BIT) may be monitored at the 1030 MHz TEST OUT port, J21, of the Interrogation Demodulation Receiver (IDR) Module. This connector is a type BNC. When not in use this test port should be terminated with the external 50 Ohm load.

Refer to the IDR Module Test Ports section for additional information on the use of IDR test output signals.

Table 22. J21 – 1030 MHz RF Interrogation Test Out

Connector Name	1030 MHz RF Test Out
Connector Reference Designator	J21
Connector Location	IDR Module Front Panel
Connector Type	BNC
VSWR/Impedance	1.5:1, 50 Ohm
Input Level	Not Applicable
Output Level	Channel A or B: 30 dB below the level of the applied input signal, -45 dBm to -10 dBm, nominal Sum Channel A or B: 55 dB below the level of the applied input signal, -45 dBm to -10 dBm, nominal BIT: 20 dB below the level of the applied BIT signal
Signal Frequency	1030 MHz

4.2.2.4 J22, J23, and J24 – Interrogation Data Test Outputs

Demodulated interrogation data may be monitored at PAM (J22), DPSK (J23), and Log Video (J24) test ports on the front panel of the Interrogation Demodulation Receiver (IDR) Module. When not in use these test ports should be terminated with the supplied 50 Ohm load (J24) or dust cover (J22 and J23).

Refer to Figure 2 for the front panel module locations.

Specifications for each of the connectors can be found in the following tables:

Figure 53

Table 23. J22 – PAM Video Test Out

Connector Name	PAM Video Test Out
Connector Reference Designator	J22
Connector Location	IDR Module Front Panel
Connector Type	BNC
VSWR/Impedance	75 Ohm
Output Level	TTL
Data Type	Demodulated PAM from the selected interrogation signal
Data Rate	At the rate of the applied interrogation pulse sequence

Table 24. J23 – DPSK Video Test Out

Connector Name	DPSK Video Test Out
Connector Reference Designator	J23
Connector Location	IDR Module Front Panel
Connector Type	BNC
VSWR/Impedance	75 Ohm
Output Level	TTL
Data Type	Demodulated DPSK from the selected interrogation signal. Applicable only to Mode S interrogations.
Data Rate	4 Mbits/second

Table 25. J24 – Log Video Test Out

Connector Name	Log Video Test Out
Connector Reference Designator	J24
Connector Location	IDR Module Front Panel
Connector Type	BNC
VSWR/Impedance	1.5:1, 50 Ohm
Output Level	Log video representation of peak pulsed power level of RF input Interrogation signal; approximately +1.4 Volts @-15 dBm in, 2.0 Volts @+20 dBm in
Data Rate	At the rate of applied interrogation pulse sequence

4.2.2.5 J25 – 1060 MHz Test Output

1060 MHz test and alignment signals are available at the Reference Source Module TEST OUT CW connector (J25). J25 is a type N connector.

Table 26. J25 – 1060 MHz Test Output

Connector Name	1060 MHz Test Out
Connector Reference Designator	J25
Connector Location	Reference Source Module Front Panel
Connector Type	N
VSWR/Impedance	1.5:1, 50 Ohm
Input Level	Not Applicable
Output Level	Operator selectable, -22 to +8 dBm The signal is only available when operating in the 1060 MHz CW Mode.
Signal Frequency	1060 MHz

4.2.2.6 J26 - 70 MHz Test Output

70 MHz IF test signals are available at the front panel of each of the three Upconverter Modules. The output signal type, Delta, Sum, or Omni, is determined by the location of the Upconverter Module in the MBTS chassis. ***It is important to terminate this port with the included 50 Ohm load when it is not in use***.

Table 27. J26 – 70 MHz Test Output Connector

Connector Name	70 MHz Test Out
Connector Reference Designator	J26
Connector Location	On each of the three Upconverter Module front panels (Sum, Delta, or Omni)
Connector Type	BNC
VSWR/Impedance	1.5:1, 50 Ohm
Output Level	Approximately 15 dB below the level of signals at the applicable Sum, Omni, or Delta Channel rear panel output
Signal Frequency	70 MHz, nominal

4.2.2.7 J27 & J28 – 1090 MHz Test Outputs

1090 MHz, Channel A and Channel B test signals may be monitored at the front panel of each of the three Upconverter Modules. The Output Select control selects which of the two test ports is active. Terminate these ports, using the attached 50 Ohm loads, when they are not in use.

Table 28. J27 & J28 – 1090 MHz Target Reply Test Outputs

Connector Name	1090 MHz Test Out
Connector Reference Designator	J27, Channel A J28, Channel B
Connector Location	On each of the three Upconverter Module front panels (Sum, Delta, or Omni)
Connector Type	BNC
VSWR/Impedance	1.5:1, 50 Ohm
Output Level	Approximately 20 dB below the level of signals at the applicable Sum, Omni, or Delta Channel rear panel output
Signal Frequency	1090 MHz nominal, Operator selectable, 1080 to 1100 MHz in 200 kHz steps

5 MAINTENANCE AND REPAIR

5.1 Periodic Maintenance

Periodically the physical condition and the electrical performance of the MBTS should be verified. Maintenance schedules should be based upon the environment in which the MBTS operates. If the MBTS is used in a hot and dusty environment maintenance should occur much more frequently than suggested below.

5.1.1 MBTS Cleaning

The physical condition of the MBTS should be inspected at a minimum of every six months for the accumulation of dust or dirt in the ventilation holes on the bottom and top panels of the chassis.

If it is found that the top or bottom panels have an accumulation of dust, it is recommended that they be cleaned with a clean, soft bristle brush, and a vacuum cleaner.

Each Upconverter Module should also be pulled out at this time to check for the accumulation of dust on their top and bottom panels. Module removal requires the use of a small flat-blade screwdriver. Each module is held in place with either two or four captive screws. Loosen the screws and pull the module away from the chassis through the use of the front panel handle. All modules should be removed if the Upconverter modules are found to be dirty. Clean these with a soft brush and vacuum cleaner, as required.

NOTE

The location of each Upconverter Module in the chassis should be noted prior to removal. Insert each Upconverter Module back into the slot from which it was extracted. Failure to do so will require realignment and possibly recalibration of the MBTS.

The chassis interior, especially the fan blades, should be thoroughly cleaned using a soft brush and vacuum cleaner.

When replacing a module use caution not to over tighten the screws that hold the module to the chassis.

If the exterior of the MBTS should require additional cleaning, it can be wiped with a clean cloth that has been moistened with a spray type of household cleaner. Do not spray the cleaner directly on the MBTS surfaces.

5.1.2 Output Level Calibration

It is recommended that the output level of the MBTS be verified at least yearly. The output level accuracy of the MBTS should be verified, either manually or automatically through the use of the process described in Section 2.3.5.3, prior to calibrating the MBTS. If the measurement results are satisfactory do not recalibrate the MBTS.

If calibration of the MBTS is required, the process is described in the Absolute Output Power Calibration Mode section of this manual. Read and thoroughly understand this information before attempting to recalibrate the MBTS.

5.2 Repair

The MBTS includes extensive Built In Test features that can often, through proper analysis, pinpoint a performance issue to a particular circuit within a particular module. Some MBTS performance parameters are continuously monitored. These are displayed on the OCS control panel as described in System Status section of this manual. Other performance parameters are checked only when the MBTS Standby/Diagnostics Mode has been selected. If the MBTS has operational issues, use the Standby/Diagnostics Mode to evaluate the problem.

Once the results of the tests performed in the Standby/Diagnostics Mode are available they can be analyzed using the outline provided in the following section. The analysis process takes into account that often a problem within a single circuit of a given module will also cause a test fault to be detected in the circuits of another module. For instance, a faulty cable between the Delta signal output of the Reply Generator and the Delta Upconverter Module will cause two fault indications. One for the Delta/Sum attenuator of the Reply Generator Module, and one for the attenuator section in the Delta channel Upconverter. This happens because the Delta channel signal from the Reply Generator is used to verify the operation of the circuits within the Delta Channel Upconverter.

The BIT process assumes that the BIT Module functions properly. The BIT Module measures the performance of all Reply Generator and Upconverter RF control circuits, and generates interrogation signals to evaluate the IDR Module. Also, signals from the Reply Generator Module are used to evaluate the performance of circuits within each Upconverter Module. This factor may produce the test results noted above.

BIT testing insures the functionality, not the absolute accuracy, of each RF control. For the MBTS design, soft failures, in which a circuit partially works, are not a likely event.

Always verify the results of the BIT process, by repeating the test sequence or through the use of external test equipment, before proceeding with module or unit replacement.

5.2.1 Trouble Diagnostics

Use the table below and the test results of the Standby/Diagnostics Mode to determine the most likely source of any problem. The Standby/Diagnostics Mode Status Indicators section of this manual defines all of the trouble conditions listed below.

Refer to Section 5.3, below, for information regarding replacement of MBTS modules.

A thorough understanding of the MBTS theory of operation, Section 3.1, will provide great insight into the trouble shooting process. This should be reviewed as necessary.

Table 29. Trouble Diagnostics - MBTS Operation

Indicated Problem	Problem Area	Suggestions
REF PLL alone or if any other PLL indicators active	Reference Source Module If no other PLL issues indicated, the LO circuit is problematic. If multiple PLL faults indicated, the crystal oscillator or output buffer is problematic.	Replace Reference Source Module
RGC PLL	Reply Generator Module PLL circuit If no other PLL issues indicated This condition may cause many other fault conditions	Replace Reply Generator Module Check Reference Signal into the module
IDR_PLL	IDR Module PLL circuit If no other PLL issues indicated	Replace IDR Module Check Reference Signal into the module
1100BIT PLL	BIT Module 1100 MHz PLL circuit If no other PLL issues indicated	Replace BIT Module Check Reference Signal into the module
70BIT PLL	BIT Module 70 MHz PLL circuit If no other PLL issues indicated	Replace BIT Module Check Reference Signal into the module
BIT Pwr Alarm	One of the three power supply voltages is non-compliant This condition may cause many other fault conditions	Check displayed power supply voltage measurements Replace appropriate Power Supply

Indicated Problem	Problem Area	Suggestions
BIT Temp Alarm	Internal temperature of MBTS is out-of-specification	Turn off MBTS. Do not operate until ambient conditions are within +10ºC and +50ºC.
Cal Failed	MBTS output level could not be properly calibrated MBTS may operate but not with specified output level accuracy	Check ambient temperature Check MBTS Calibration (see Section 5.1.2)
Fan Failed	Fan has stopped rotating	Replace Fan Check wiring to Fan The MBTS should not be operated for more than fifteen minutes at a time with this failure
ANT ROT Alarm	The antenna rotation rate is higher or lower than expected	Check the APG Input selection Check the APG signals into the MBTS Turn off the Antenna Alarm
APG Alarm	Data from the APG source is not as required	Check the APG Input selection Check the APG signals into the MBTS Turn off Antenna Alarm
DUP Atten	Attenuator circuit within the Delta Channel Upconverter	Note if ADS Atten fault exists. If so check this fault first Replace Delta Channel Upconverter
OUP Atten	Attenuator circuit within the Omni Channel Upconverter	Note if TGT Atten fault exists. If so check this fault first Replace Omni Channel Upconverter
SUP Atten	Attenuator circuit within the Sum Channel Upconverter	Note if SO Atten fault exists. If so check this fault first Replace Sum Channel Upconverter

Indicated Problem	Problem Area	Suggestions
TGT Atten	Target Level Attenuator circuit within the Reply Generator This condition may cause many other fault conditions	A) Verify attenuator performance at the Omni Upconverter 70 MHz test port Replace the Reply Generator Module B) Verify 32 dB gain step in Sum Channel Upconverter Replace the Reply Generator Module
SO Atten	Sum/Omni Attenuator circuit within the Reply Generator This condition may cause many other fault conditions (TGT Atten and OUP Atten may be OK)	Verify attenuator performance at the Sum Upconverter 70 MHz test port Replace the Reply Generator Module
DS Atten	Delta/Sum Attenuator circuit within the Reply Generator This condition may cause many other fault conditions (TGT Atten, OUP Atten, SO Atten, and SUP Atten may be OK)	Verify attenuator performance at the Sum Upconverter 70 MHz test port Replace the Reply Generator Module
ADS Atten	Aux Delta/Sum Attenuator within the Reply Generator Applies to the Sum and Omni channels outputs	Verify which attenuator section is faulty; at the Sum Upconverter 70 MHz test port, or Omni Upconverter 70 MHz test port Replace the Reply Generator Module
Phase Modulator	Phase Modulator circuit within the Reply Generator Module	Check Delta/Sum phase at output of MBTS Replace the Reply Generator Module
PAM Atten	Pulse Amplitude Modulator circuit within the Reply Generator Module	Check operation of circuit at rear panel of MBTS Replace the Reply Generator Module

Indicated Problem	Problem Area	Suggestions
XILINX Load Bad	Xilinx or Flash ROM of PCC Module	Reprogram Flash ROM of PCC Module Replace PCC Module
Flash CAL Bad	Flash ROM of PCC Module	Reprogram Flash ROM of PCC Module Replace PCC Module
BER Reply Fail	Should never be problematic	Rerun test process
BER Inter Fail	Interrogation Demodulation Circuits	Check IDR data outputs Replace IDR Module Check PCC operation with Mode Pair Triggers Replace PCC Module
XILINX Bad	Xilinx used in PCC Module	Replace PCC Module
Cal Flash Bad	Flash ROM of PCC Module	Retest Reprogram Flash ROM Replace PCC Module
Prog ROM Bad	Flash ROM of PCC Module	Retest Reprogram Flash ROM Replace PCC Module

5.3 Module Replacement

Replacing, instead of repairing, a faulty module is a valid maintenance strategy if the following limitations are understood and can be overcome.

The performance of every production module is slightly different. Gain and phase variations within Reply Generator Modules and Upconverter Modules, in particular, are of major importance. These differences are equalized, at the factory, through the use of calibration constants stored in the PCC Module. Therefore the replacement of any of these three modules, the Reply Generator, the Upconverter, or the PCC, may result in less than specified performance. It is recommended that the MBTS unit be returned to the factory, in its original configuration, if diagnostics indicate that any of these three modules are found to be faulty.

All other MBTS modules may be replaced without concern for the above issues. These include the BIT Module, the IDR Module, and the Reference Source Module.

Module removal requires the use of a small flat-blade screwdriver. Each module is held in place with either two or four captive screws. Loosen the screws and pull the module away from the chassis through the use of the front panel handle. When replacing the module use caution not to over tighten the screws that hold the module to the chassis.

6 INSTALLATION, INTEGRATION, AND CHECKOUT

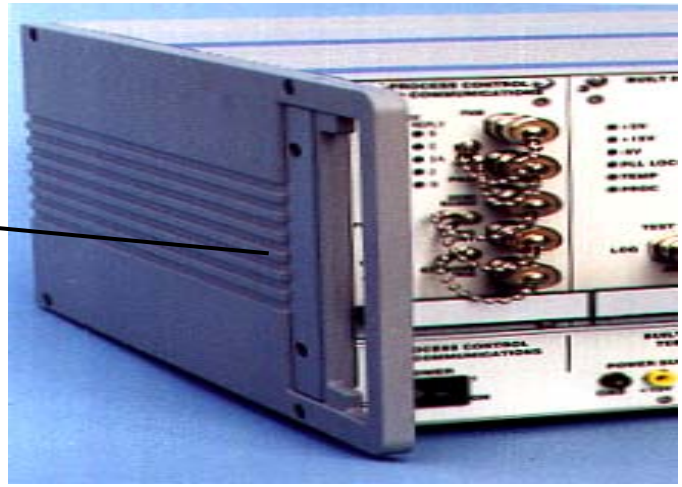
6.1 Installation

The MBTS can be operated from a tabletop or it can be installed in a standard 19-inch equipment rack.

If operated on a tabletop, the chassis bottom and top must be clear of any obstructions so as to allow proper ventilation.

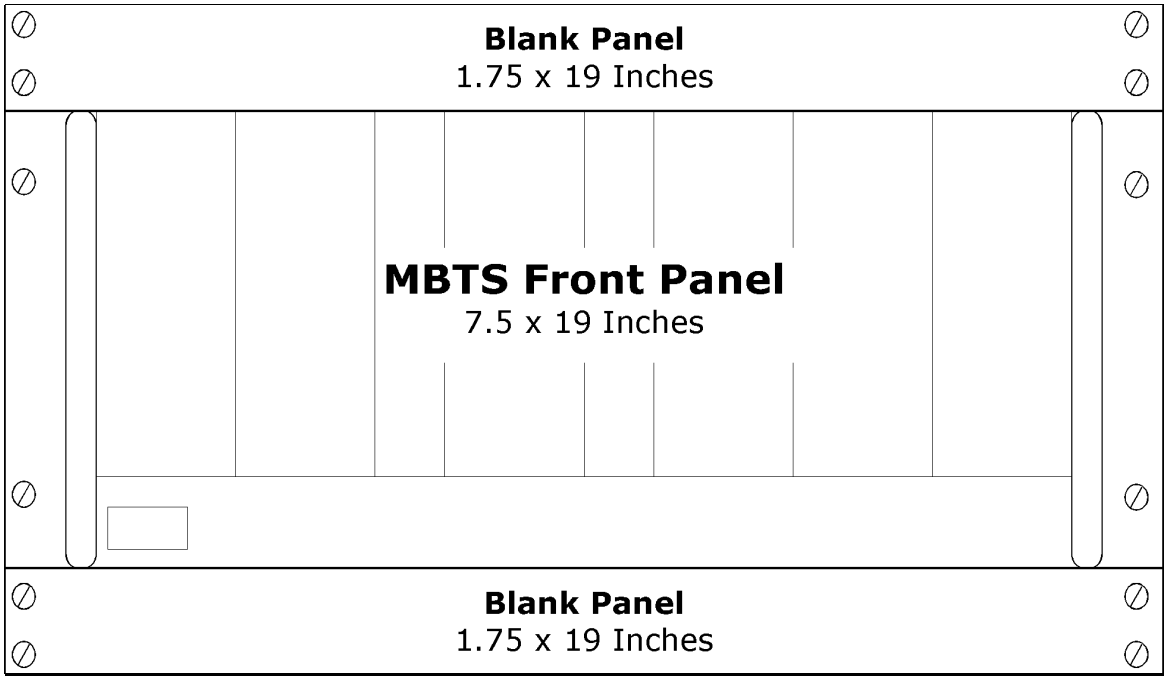
Hinged brackets for mounting in a standard EIA/RETMA 19-inch equipment rack or cabinet are included as part of the chassis as shown below in Figure 56. The brackets are shown in the retracted position. They can be easily extended to a right angle from the chassis.

Figure 56. MBTS Chassis Rack Mount Brackets



The MBTS front panel is 7.5 inches high, but a minimum opening of 10.5 inches is recommended for mounting it within an equipment rack or cabinet. As shown in Figure 57 below, 1.75 inch high blank panels should be mounted above and below the chassis to allow adequate air flow through the MBTS.

Figure 57. Recommended Rack Mount Configuration



6.2 Integration

The MBTS system consists of the MBTS, an Operator Control Subsystem (OCS), phase-matched RF cable sets, and an azimuth data cable. The OCS consists of a laptop Pentium computer configured with MBTS control software and an IEEE-488 interface. Refer to Section 2.0, System Operation, for information on starting and operating the MBTS and OCS.

To integrate the MBTS with a radar system review the operational characteristics and requirements of the radar system and of the MBTS. Use Figure 1, the MBTS System Block Diagram, and Figure 29, the Azimuth Gated Target Mode Block Diagram, to assist in planning the interconnects to the radar system. Information included in related text, such as found in Section 2.3.3.2, Azimuth Gated Target Mode Connections, will also be useful. Refer to Figure 3 for rear panel connector locations.

Two sets of phase-matched cables are delivered with the MBTS system. Each set consists of three twenty-five foot long cables. The cables of each set should be attached to a single channel of Sum, Omni, and Delta outputs at the rear panel of the MBTS. Do not mix the cables of the two sets between the outputs of the different channels. The attachment point of the other end of the phase matched RF cables is radar system dependent. For the ATCBI-6 radar, however, this connection is usually made at the coupled port of the 20dB dual directional coupler located at the top of the transmit/receive cabinet. ***Consult with the site engineer to verify the location of all signal connections***.

The MBTS operates on 115/230 VAC 50-60 Hz power. This should be provided at J14 - AC Power Input Connector.

APG signals from the radar system antenna pedestal must be connected to the MBTS. Use either the balanced APG input connection, at J9 – RS-422 Antenna Azimuth Data Inputs, or the unbalanced APG input connections J10 – 75 Ohm Azimuth ACP Input and J11 - 75 Ohm Azimuth ARP Input. A 25-foot APG interface cable is provided with the MBTS System to connect signals from the APG outputs of a radar system to the balanced inputs of the MBTS. A special APG adapter cable is also provided with MBTS Systems delivered to ASR-11 equipped radar sites. Attach this adapter cable to the free end of the 25-foot APG cable and to the APG outputs of the ASR-11.

The MBTS and OCS communicate through an IEEE-488 interface. Information regarding the configuration of this link is found in Section 2.1.2, GPIB Address Setup. The OCS computer includes a PCMCIA IEEE-488 adapter and cable. Use these to make the physical connection to the MBTS at rear panel connector J12.

6.2.1 System Phase Matching

For the MBTS to work properly with the radar system, the signals from the Delta and Sum outputs must exhibit the correct phase properties at the radar inputs. Consult with the site engineer as to signal phase requirements. Phase adjustment devices, one for each Delta signal channel, provide the means to alter the phase of MBTS outputs to meet system requirements. See Section 3.3.1.3, Sum/Delta Phase Adjust, for more information. Ninety-degree phase adapter cables, one for each RF channel, are also provided with the MBTS system for this purpose.

To set the phase relationship of the Sum and Delta channel signals, first disconnect the phase matched cables from the signal coupler located at or near the radar transmitter/receiver (if not already disconnected). Connect the cables to a Vector Voltmeter (such as an HP 8508) using the Sum Channel output signal from the MBTS as the reference. Operate the MBTS in CW Mode.

Set the Sum RF Level signal level of the MBTS to 0 dBm. Set the D/S Ratio to –20 dB. Enable the RF output (either Channel A or B as appropriate). Monitor the Sum/Delta phase relationship as displayed by the Vector Voltmeter while varying the phase adjustment device appropriate for the signal channel in use. Set the Sum/Delta relationship as required. Use the 90º adapter cables if necessary. Once the proper phase relationship has been established place the MBTS into the desired operational state, usually either Constant Range Ring Mode or Azimuth Gated Target Mode. The MBTS may now be reconnected to the radar system.

Signal phasing issues are demonstrated when responses generated by the MBTS, and as displayed on the radar target screen, appear as splits around a single target azimuth, or are transitory – are displayed on one, but not all sweeps, of the radar. Note that this condition is similar to when the MBTS is set for a low output signal level.

To verify MBTS operation and proper signal phasing operate the MBTS in the Azimuth Gated Target Mode.

With the MBTS output enabled observe the targets as displayed on the radar screen. Eight MBTS generated targets should be displayed equally spaced around the 50-mile range circle. Consult with the site engineer as to the availability of procedures to further verify the operation of the MBTS.

6.2.2 Antenna Pattern Calibration

To optimize its output characteristics, the MBTS should be calibrated to match the characteristics of the antenna used by the radar system. To begin this process, place the MBTS into the Off-Boresight Calibration Mode (refer to Section 2.3.4). Be sure to follow the system configuration guidelines provided in this section. When in the Off-Boresight Calibration Mode the MBTS generates pulsed RF replies in which the monopulse setting of a reply sequence is encoded

into the reply data transmission. The reply data from the MBTS is recorded and analyzed by the radar system. Consult with the site engineer for procedures and processes for setting the radar for data collection, data analysis, and to generate a new Boresight antenna file. Software to analyze MBTS signals received by the radar system is not provided with the MBTS system.

A new Boresight file is created as a result of the analysis process (a new Beamshape file may also be created but is not an absolute necessity). The format of the Boresight file should comply with the structure defined by the BORESIGHT command in the MBTS IEEE-488 COMMAND SET document (FSE Drawing Number 100606). The file should be placed at a convenient location on the OCS computer.

The new Boresight file is then loaded into the MBTS. To do this, place the MBTS into the Cal Settings/Antenna Patterns Mode. Activate the Upload Ant Boresight control. Find and select the Boresight file previously placed on the OCS computer. The file transfer is then made automatically. Verify the Boresight pattern by selecting the View Current Setting control and then reviewing the displayed Boresight information. When operating the MBTS in Azimuth Gated Target Mode make sure that the User antenna pattern is selected.